



Q87H3-AD2 Rev:1.0

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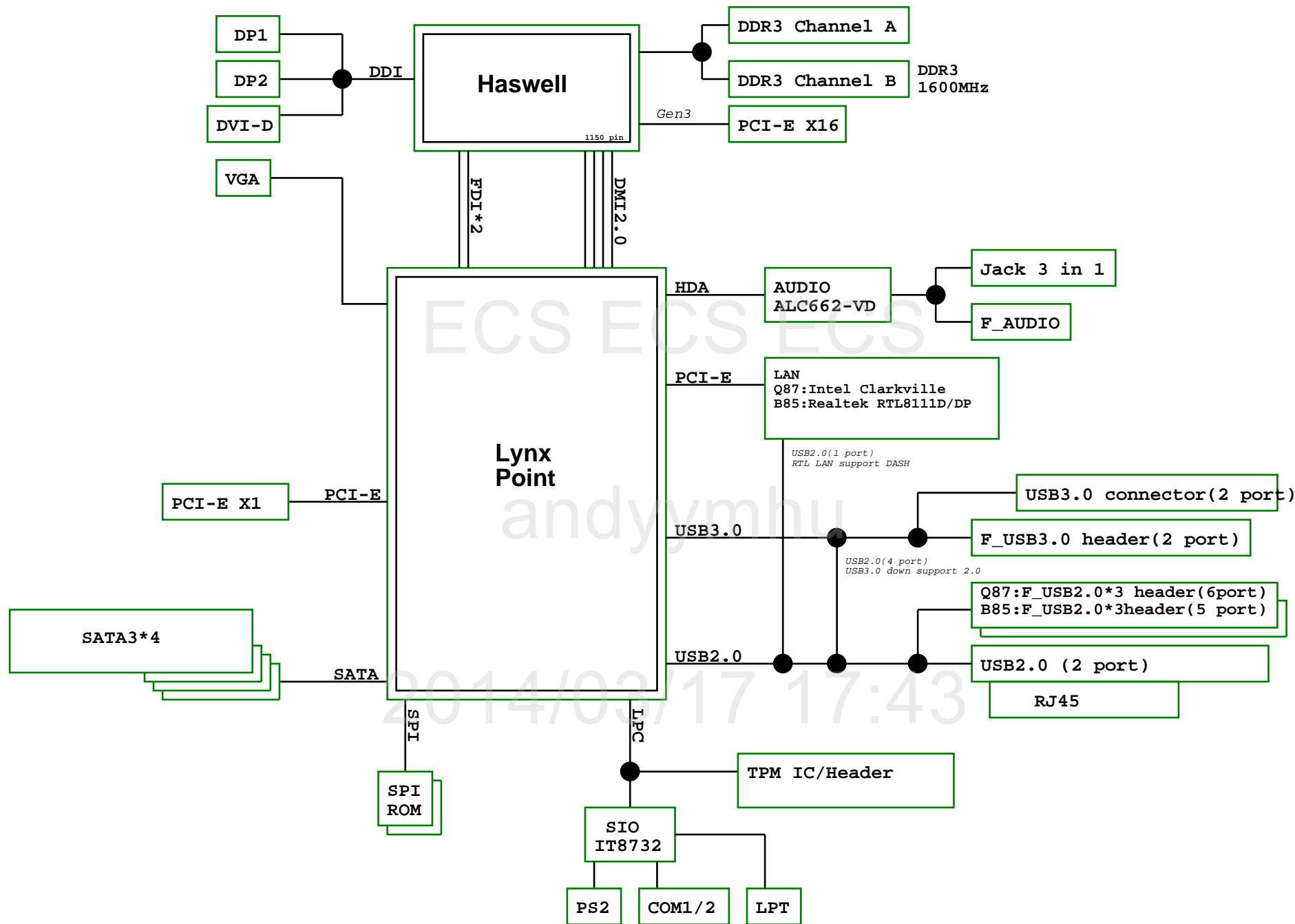
TABLE OF CONTENTS

Page	Index
1	Cover Page
2	Block Diagram
3	GPIO Function & INT# Mapping
4	CPU-PEG/DMI/FDI/DDI
5	CPU-MISC
6	CPU-DDR3
7	CPU-POWER
8	CPU-GND
9	PCIE*16
10	DP1/DP2
11	DVI-D+VGA
12	DDR3-CHA
13	DDR3-CHB
14	DDR3-Vref
15	PCH-DMI/PE/USB2.0
16	PCH-FDI/DDI/USB3.0/CLK
17	PCH-SATA/SATA CONN & PWR/OBR
18	PCH-MISC
19	PCH-POWER
20	PCH-GND
21	PCIE*1
22	USB2.0 Header
23	USB3.0 Header
24	SPI/SMbus
25	ECIO-IT8732
26	FAN/PS2/Buzzer/F_Panel
27	LPT/COM/TPM

REVISION HISTORY:

Rev	Date	Notes
A		
1.0		

Title Cover Page		
Size Custom	Document Number Q87H3-AD2	Rev 1.0
Date: Monday, March 17, 2014	Sheet 1	of 40



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	ME_Disable	GPO
GPIO40	3VSB	USB_EN	Native
GPIO45	3VSB	BIOS_WP	Native
GPIO57	3VSB	BIOS_WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL, BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRRX2
GP36	3VSB	Thermal_SD	PWMOUT
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPIO
GP71	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP76	VCC3	Thermal_HD_Auto_Switch	GPIO
GP46	3VSB	Acer Header	GPIO
GP47	3VSB	Acer Header	GPIO
GP40	3VSB	5VDUAL Switch	3VSB

BIOS must be pro to Native 3VSB

Interrupt mapping

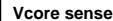
Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
SATA	INTB#	NA	LPT integrate


Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
Q87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3	SATA 6Gb/s Port 4
Q85	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 3Gb/s Port 1	SATA 3Gb/s Port 2	SATA 6Gb/s Port 3	SATA 6Gb/s Port 4
B85	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 3Gb/s Port 1	SATA 3Gb/s Port 2	SATA 6Gb/s Port 3	SATA 6Gb/s Port 4
Z87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3	SATA 6Gb/s Port 4
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3	SATA 6Gb/s Port 4
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	NA	NA	SATA 3Gb/s Port 1	SATA 3Gb/s Port 2	SATA 6Gb/s Port 3	NA	NA

Table 1-2. Desktop Lynx Point SKUs

Feature Set	SKU Name					
	Intel® Q87 Express Chipset	Intel® Q85 Express Chipset	Intel® B85 Express Chipset	Intel® Z87 Express Chipset	Intel® H87 Express Chipset	Intel® H81 Express Chipset
Flexible I/O	Yes	No	No	Yes	Yes	No
PCI Express* 2.0 Ports	8 ⁴	8	8	8 ⁴	8 ⁴	6
Total number of USB ports	14	14	12 ⁵	14	14	10 ⁶
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4(6) ⁷	4	4	4(6) ⁷	4(6) ⁷	2 ⁸
• USB 2.0 Only Ports	10(8) ⁹	10	8	10(8) ⁹	10(8) ⁹	8
Total number of SATA ports	4(6) ¹⁰	6	6	4(6) ¹⁰	4(6) ¹⁰	4 ¹¹
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	6	4 ¹²	4 ¹²	6	6	2 ¹³
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	0	2	2	0	0	2
VGA	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	No	No	Yes	No
	Intel® Smart Response Technology ¹⁴	Yes	No	No	Yes	No
Intel® Anti-Theft Technology ¹⁵	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 9.0	Yes	No	No	No	No	No
Intel® Small Business Advantage ¹⁶	Yes	Yes	Yes	No	Yes ¹⁷	No
Intel Rapid Start Technology ¹⁸	Yes	Yes	Yes	Yes	Yes	No
Intel® Identity Protection Technology (Intel® IPT) ¹⁹	Yes	No	No	No	No	No
Near Field Communication ²⁰	Yes	Yes	Yes	Yes	Yes	Yes
ACPI S1 State Support	Yes	Yes	Yes	Yes	Yes	Yes



			
Title CPU-MISC			
Size	Document Number		Rev
Custom	Q87H3-AD2		1.0
Date:	Monday, March 17, 2014	Sheet	5 of 40

12	M_DATA_A[0..63]	← M_DATA A[0..63]
12	M_DQS_A_P[0..7]	← M_DQS A P[0..7]
12	M_DQS_A_N[0..7]	← M_DQS A N[0..7]
12	M_MA_A[0..15]	← M_MA A[0..15]
12	M_BS_A[0..2]	← M_BS A[0..2]
12	M_CS_A_L[0..3]	← M_CS A L[0..3]
12	M_CKE_A[0..3]	← M_CKE A[0..3]
12	M_ODT_A[0..3]	← M_ODT A[0..3]
12	M_CLK_A_P[0..3]	← M_CLK A P[0..3]
12	M_CLK_A_N[0..3]	← M_CLK A N[0..3]
12	M_WE_A_L	← M_WE A L
12	M_CAS_A_L	← M_CAS A L
12	M_RAS_A_L	← M_RAS A L

DDR3 CH.A

13	M_DATA_B[0..63]	← M_DATA B[0..63]
13	M_DQS_B_P[0..7]	← M_DQS B P[0..7]
13	M_DQS_B_N[0..7]	← M_DQS B N[0..7]
13	M_MA_B[0..15]	← M_MA B[0..15]
13	M_BS_B[0..2]	← M_BS B[0..2]
13	M_CS_B_L[0..3]	← M_CS B L[0..3]
13	M_CKE_B[0..3]	← M_CKE B[0..3]
13	M_ODT_B[0..3]	← M_ODT B[0..3]
13	M_CLK_B_P[0..3]	← M_CLK B P[0..3]
13	M_CLK_B_N[0..3]	← M_CLK B N[0..3]
13	M_WE_B_L	← M_WE B L
13	M_CAS_B_L	← M_CAS B L
13	M_RAS_B_L	← M_RAS B L

DDR3 CH.B

6,12,13 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

**Attention

M_DATA A0	AD38	SA_DQ[0]
M_DATA A1	AD39	SA_DQ[1]
M_DATA A2	AF38	SA_DQ[2]
M_DATA A3	AF39	SA_DQ[3]
M_DATA A4	AD37	SA_DQ[4]
M_DATA A5	AD40	SA_DQ[5]
M_DATA A6	AF37	SA_DQ[6]
M_DATA A7	AF40	SA_DQ[7]
M_DATA A8	AH40	SA_DQ[8]
M_DATA A9	AH39	SA_DQ[9]
M_DATA A10	AK38	SA_DQ[10]
M_DATA A11	AK39	SA_DQ[11]
M_DATA A12	AH37	SA_DQ[12]
M_DATA A13	AH38	SA_DQ[13]
M_DATA A14	AK37	SA_DQ[14]
M_DATA A15	AK40	SA_DQ[15]
M_DATA A16	AM40	SA_DQ[16]
M_DATA A17	AM39	SA_DQ[17]
M_DATA A18	AP38	SA_DQ[18]
M_DATA A19	AP39	SA_DQ[19]
M_DATA A20	AM37	SA_DQ[20]
M_DATA A21	AM38	SA_DQ[21]
M_DATA A22	AP37	SA_DQ[22]
M_DATA A23	AP40	SA_DQ[23]
M_DATA A24	AV37	SA_DQ[24]
M_DATA A25	AW37	SA_DQ[25]
M_DATA A26	AW38	SA_DQ[26]
M_DATA A27	AV35	SA_DQ[27]
M_DATA A28	AT37	SA_DQ[28]
M_DATA A29	AU37	SA_DQ[29]
M_DATA A30	AT35	SA_DQ[30]
M_DATA A31	AW35	SA_DQ[31]
M_DATA A32	AV36	SA_DQ[32]
M_DATA A33	AU36	SA_DQ[33]
M_DATA A34	AV4	SA_DQ[34]
M_DATA A35	AU4	SA_DQ[35]
M_DATA A36	AV6	SA_DQ[36]
M_DATA A37	AV6	SA_DQ[37]
M_DATA A38	AW4	SA_DQ[38]
M_DATA A39	AY4	SA_DQ[39]
M_DATA A40	AR1	SA_DQ[40]
M_DATA A41	AR4	SA_DQ[41]
M_DATA A42	AN3	SA_DQ[42]
M_DATA A43	AN4	SA_DQ[43]
M_DATA A44	AR2	SA_DQ[44]
M_DATA A45	AR3	SA_DQ[45]
M_DATA A46	AN2	SA_DQ[46]
M_DATA A47	AN1	SA_DQ[47]
M_DATA A48	AL1	SA_DQ[48]
M_DATA A49	AL4	SA_DQ[49]
M_DATA A50	AJ3	SA_DQ[50]
M_DATA A51	AJ4	SA_DQ[51]
M_DATA A52	AL2	SA_DQ[52]
M_DATA A53	AL3	SA_DQ[53]
M_DATA A54	AJ2	SA_DQ[54]
M_DATA A55	AJ1	SA_DQ[55]
M_DATA A56	AG1	SA_DQ[56]
M_DATA A57	AG4	SA_DQ[57]
M_DATA A58	AE3	SA_DQ[58]
M_DATA A59	AE4	SA_DQ[59]
M_DATA A60	AG2	SA_DQ[60]
M_DATA A61	AG3	SA_DQ[61]
M_DATA A62	AE2	SA_DQ[62]
M_DATA A63	AE1	SA_DQ[63]
M_DQS A P0	AE39	SA_DQS[0]
M_DQS A P1	AN39	SA_DQS[1]
M_DQS A P2	AN38	SA_DQS[2]
M_DQS A P3	AV36	SA_DQS[3]
M_DQS A P4	AV5	SA_DQS[4]
M_DQS A P5	AP3	SA_DQS[5]
M_DQS A P6	AK3	SA_DQS[6]
M_DQS A P7	AF3	SA_DQS[7]
M_DQS A N0	AE38	SA_DQS[8]
M_DQS A N1	AJ38	SA_DQS[9]
M_DQS A N2	AN38	SA_DQS[10]
M_DQS A N3	AU36	SA_DQS[11]
M_DQS A N4	AV5	SA_DQS[12]
M_DQS A N5	AP2	SA_DQS[13]
M_DQS A N6	AK2	SA_DQS[14]
M_DQS A N7	AF2	SA_DQS[15]
M_DQS A N8	AU32	SA_DQS[16]

CPU1A

HASWELL

REV = 1

SA_MA[0]	AU13 M MA A0
SA_MA[1]	AV16 M MA A1
SA_MA[2]	AU16 M MA A2
SA_MA[3]	AW17 M MA A3
SA_MA[4]	AW18 M MA A5
SA_MA[5]	AV17 M MA A6
SA_MA[6]	AT18 M MA A8
SA_MA[7]	AT19 M MA A9
SA_MA[8]	AW11 M MA A10
SA_MA[9]	AV19 M MA A11
SA_MA[10]	AU19 M MA A12
SA_MA[11]	AY10 M MA A13
SA_MA[12]	AU20 M MA A14
SA_MA[13]	AU21 M MA A15
SA_MA[14]	AW10 M ODT A0
SA_MA[15]	AY8 M ODT A1
SA_ODT[0]	AW9 M ODT A2
SA_ODT[1]	AU8 M ODT A3
SA_ODT[2]	AW33
SA_ODT[3]	AV33
SA_ECC_CB[0]	AV31
SA_ECC_CB[1]	AV31
SA_ECC_CB[2]	AV31
SA_ECC_CB[3]	AV31
SA_ECC_CB[4]	AV31
SA_ECC_CB[5]	AV31
SA_ECC_CB[6]	AV31
SA_ECC_CB[7]	AV31
SA_BS[0]	AV12 M BS A0
SA_BS[1]	AV11 M BS A1
SA_BS[2]	AT21 M BS A2
SA_CKE[0]	AV22 M CKE A0
SA_CKE[1]	AT22 M CKE A2
SA_CKE[2]	AU23 M CKE A3
SA_CKE[3]	AU14 M CS A L0
SA_CS[0]	AV9 M CS A L1
SA_CS[1]	AU10 M CS A L2
SA_CS[2]	AW8 M CS A L3
SA_CS[3]	AY15 M CLK A P0
SA_CK[0]	AY16 M CLK A N0
SA_CK[1]	AW15 M CLK A P1
SA_CK[2]	AY14 M CLK A P2
SA_CK[3]	AW14 M CLK A N2
SA_CK[4]	AW13 M CLK A P3
SA_CK[5]	AY13 M CLK A N3
SA_CK[6]	AW12 CPU AW12
SA_CK[7]	TP6
RSVD_AW12	
SA_RAS	AU12 M RAS A L
SA_WE	AV20 CPU AV20
RSVD_AV20	TP5
RSVD_AW27	AW27 CPU AW27
SA_CAS	AU9 M CAS A L
SM_DRAMRST	AK22
DRAMRT	R472 0-04
DDR3_DRAMRST_L	6,12,13
C376	.1U-16VX7-04-O
GND	close to DIMM slot

HASWELL

1 OF 10

**Attention

M_DATA B0	AE34	SB_DQ[0]
M_DATA B1	AE35	SB_DQ[1]
M_DATA B2	AG35	SB_DQ[2]
M_DATA B3	AG36	SB_DQ[3]
M_DATA B4	AD34	SB_DQ[4]
M_DATA B5	AD35	SB_DQ[5]
M_DATA B6	AG34	SB_DQ[6]
M_DATA B7	AH34	SB_DQ[7]
M_DATA B8	AL34	SB_DQ[8]
M_DATA B9	AL35	SB_DQ[9]
M_DATA B10	AK31	SB_DQ[10]
M_DATA B11	AL31	SB_DQ[11]
M_DATA B12	AK34	SB_DQ[12]
M_DATA B13	AK35	SB_DQ[13]
M_DATA B14	AK32	SB_DQ[14]
M_DATA B15	AL32	SB_DQ[15]
M_DATA B16	AN34	SB_DQ[16]
M_DATA B17	AP34	SB_DQ[17]
M_DATA B18	AN31	SB_DQ[18]
M_DATA B19	AP31	SB_DQ[19]
M_DATA B20	AN35	SB_DQ[20]
M_DATA B21	AP35	SB_DQ[21]
M_DATA B22	AN32	SB_DQ[22]
M_DATA B23	AP32	SB_DQ[23]
M_DATA B24	AM28	SB_DQ[24]
M_DATA B25	AR29	SB_DQ[25]
M_DATA B26	AR28	SB_DQ[26]
M_DATA B27	AL29	SB_DQ[27]
M_DATA B28	AL28	SB_DQ[28]
M_DATA B29	AP29	SB_DQ[29]
M_DATA B30	AP29	SB_DQ[30]
M_DATA B31	AP29	SB_DQ[31]
M_DATA B32	AR12	SB_DQ[32]
M_DATA B33	AP12	SB_DQ[33]
M_DATA B34	AL13	SB_DQ[34]
M_DATA B35	AL12	SB_DQ[35]
M_DATA B36	AR13	SB_DQ[36]
M_DATA B37	AM13	SB_DQ[37]
M_DATA B38	AM13	SB_DQ[38]
M_DATA B39	AM12	SB_DQ[39]
M_DATA B40	AR9	SB_DQ[40]
M_DATA B41	AP9	SB_DQ[41]
M_DATA B42	AR6	SB_DQ[42]
M_DATA B43	AP5	SB_DQ[43]
M_DATA B44	AR10	SB_DQ[44]
M_DATA B45	AP10	SB_DQ[45]
M_DATA B46	AR7	SB_DQ[46]
M_DATA B47	AP7	SB_DQ[47]
M_DATA B48	AM7	SB_DQ[48]
M_DATA B49	AL9	SB_DQ[49]
M_DATA B50	AL6	SB_DQ[50]
M_DATA B51	AL7	SB_DQ[51]
M_DATA B52	AM10	SB_DQ[52]
M_DATA B53	AL10	SB_DQ[53]
M_DATA B54	AM5	SB_DQ[54]
M_DATA B55	AM7	SB_DQ[55]
M_DATA B56	AH6	SB_DQ[56]
M_DATA B57	AH7	SB_DQ[57]
M_DATA B58	AE6	SB_DQ[58]
M_DATA B59	AE7	SB_DQ[59]
M_DATA B60	AJ5	SB_DQ[60]
M_DATA B61	AJ7	SB_DQ[61]
M_DATA B62	AF6	SB_DQ[62]
M_DATA B63	AF7	SB_DQ[63]
M_DQS B P0	AF35	SB_DQS[0]
M_DQS B P1	AL33	SB_DQS[1]
M_DQS B P2	AP33	SB_DQS[2]
M_DQS B P3	AN28	SB_DQS[3]
M_DQS B P4	AN12	SB_DQS[4]
M_DQS B P5	AP8	SB_DQS[5]
M_DQS B P6	AL8	SB_DQS[6]
M_DQS B P7	AG1	SB_DQS[7]
M_DQS B N0	AF34	SB_DQS[8]
M_DQS B N1	AK33	SB_DQS[9]
M_DQS B N2	AN33	SB_DQS[10]
M_DQS B N3	AN29	SB_DQS[11]
M_DQS B N4	AN15	SB_DQS[12]
M_DQS B N5	AR8	SB_DQS[13]
M_DQS B N6	AM8	SB_DQS[14]
M_DQS B N7	AG6	SB_DQS[15]
M_DQS B N8	AN28	SB_DQS[16]

CPU1B

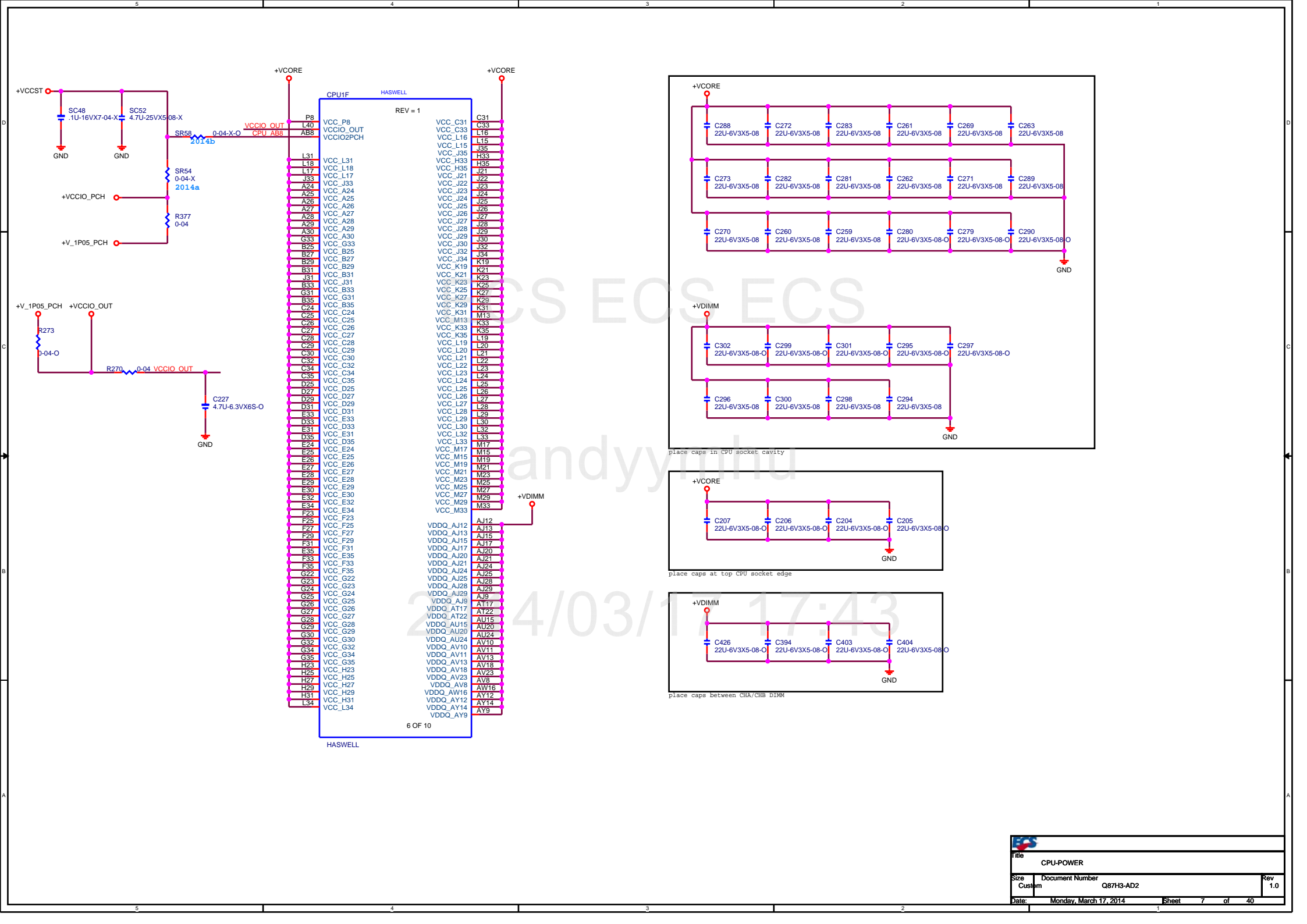
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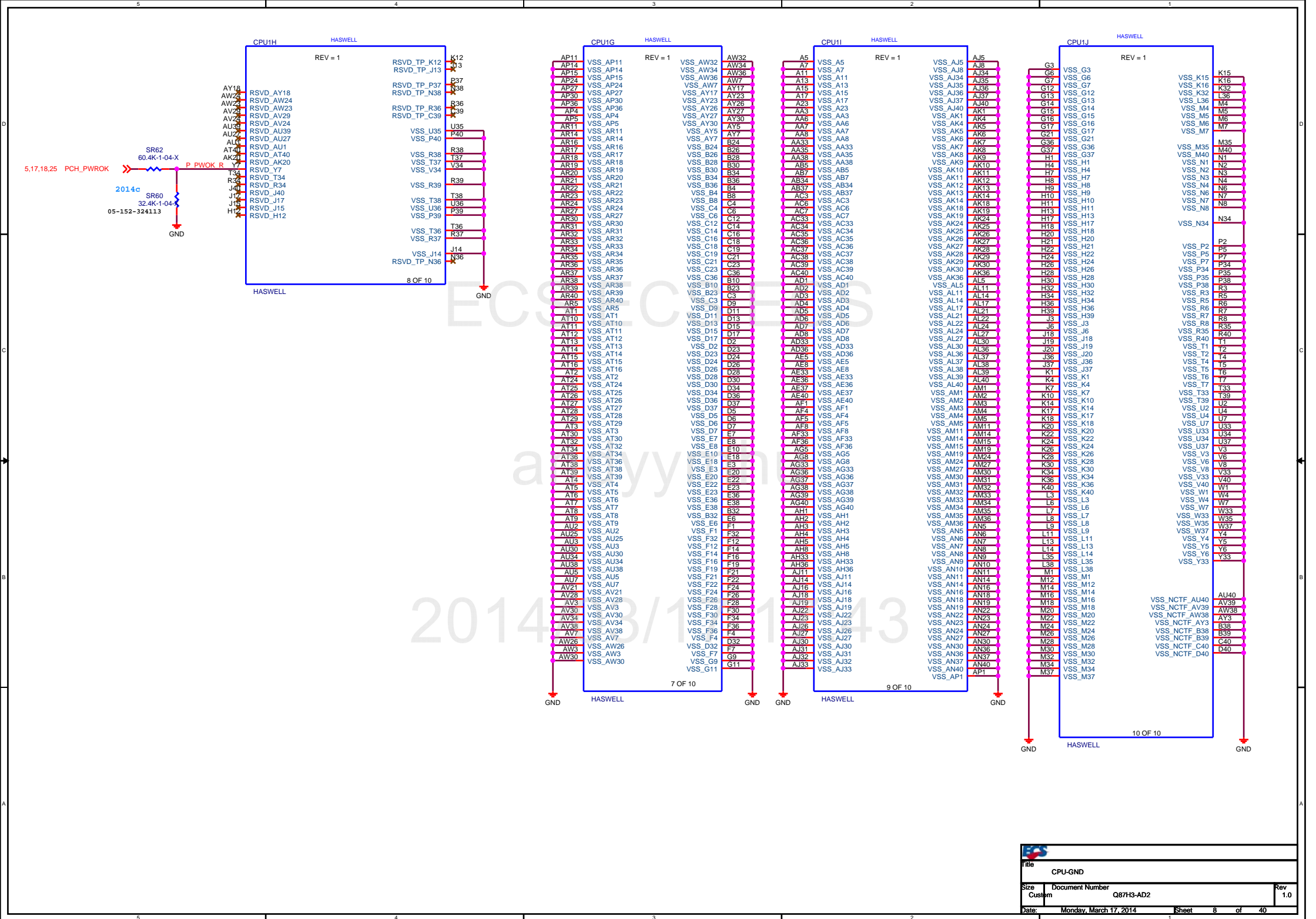
REV = 1

SB_MA[0]	AL19 M MA B0
SB_MA[1]	AK23 M MA B1
SB_MA[2]	AM22 M MA B2
SB_MA[3]	AP23 M MA B4
SB_MA[4]	AL23 M MA B5
SB_MA[5]	AY24 M MA B6
SB_MA[6]	AV25 M MA B7
SB_MA[7]	AV25 M MA B9
SB_MA[8]	AP18 M MA B10
SB_MA[9]	AY25 M MA B11
SB_MA[10]	AV26 M MA B12
SB_MA[11]	AR15 M MA B13
SB_MA[12]	AV27 M MA B14
SB_MA[13]	AY28 M MA B15
SB_MA[14]	AM17 M ODT B0
SB_MA[15]	AL16 M ODT B1
SB_ODT[0]	AM16 M ODT B2
SB_ODT[1]	AK15 M ODT B3
SB_ODT[2]	AM26
SB_ODT[3]	AM25
SB_ECC_CB[0]	AP25
SB_ECC_CB[1]	AP26
SB_ECC_CB[2]	AP26
SB_ECC_CB[3]	AP26
SB_ECC_CB[4]	AP26
SB_ECC_CB[5]	AP26
SB_ECC_CB[6]	AP25
SB_ECC_CB[7]	AK17 M BS B0
SB_BS[0]	AL18 M BS B1
SB_BS[1]	AW28 M BS B2
SB_BS[2]	AW29 M CKE B0
SB_CKE[0]	AY29 M CKE B1
SB_CKE[1]	AU28 M CKE B2
SB_CKE[2]	AU29 M CKE B3
SB_CKE[3]	AP17 M CS B L0
SB_CS[0]	AN15 M CS B L1
SB_CS[1]	AN17 M CS B L2
SB_CS[2]	AL15 M CS B L3
SB_CS[3]	AM20 M CLK B P0
SB_CK[0]	AM21 M CLK B N0
SB_CK[1]	AP22 M CLK B P1
SB_CK[2]	AP21 M CLK B N1
SB_CK[3]	AN20 M CLK B P2
SB_CK[4]	AN21 M CLK B N2
SB_CK[5]	AP19 M CLK B P3
SB_CK[6]	AP20 M CLK B N3
SB_CK[7]	AP16 M CAS B L
SB_CAS	AL20 CPU AL20
RSVD_AL20	STP15
SB_RAS	AM18 M RAS B L
SB_WE	AK16 M WE B L
SA_DIMM_VREFDQ	AB39 DIMM DQ CPU VREF A
SB_DIMM_VREFDQ	AB40 DIMM DQ CPU VREF B
C303	.022U-16VX7-04
C292	.022U-16VX7-04
R363	24.9-1-04
R360	24.9-1-04
GNDGND	

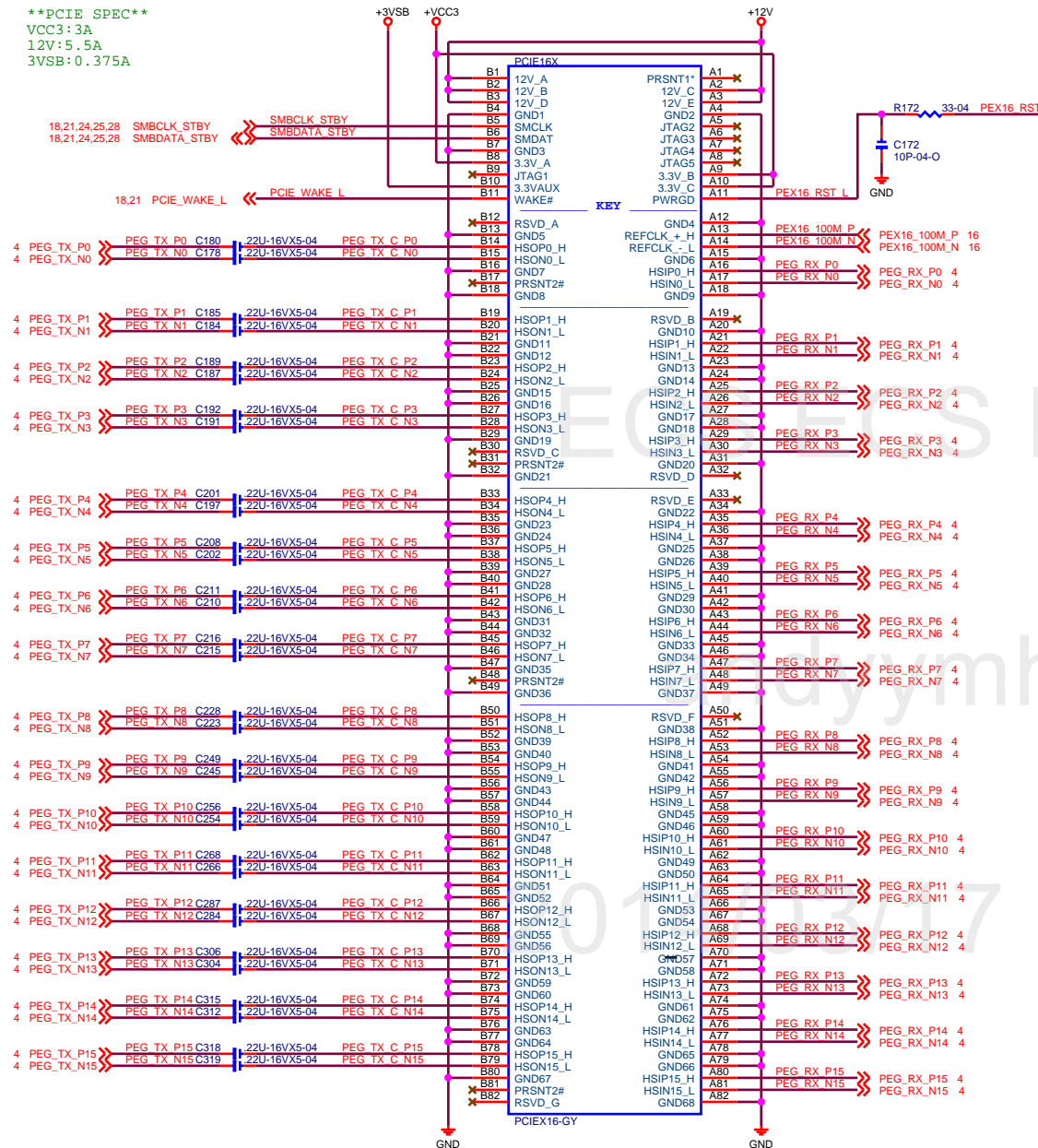
HASWELL

2 OF 10

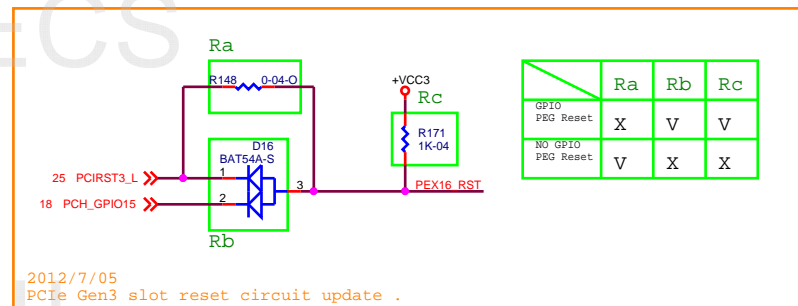
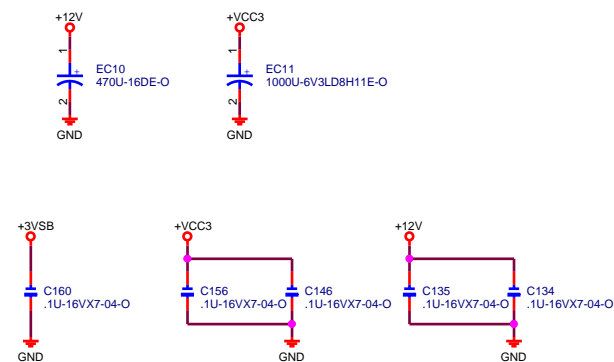


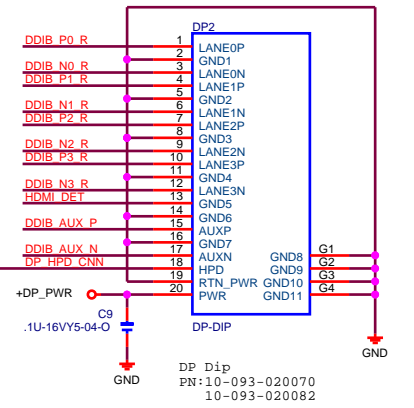
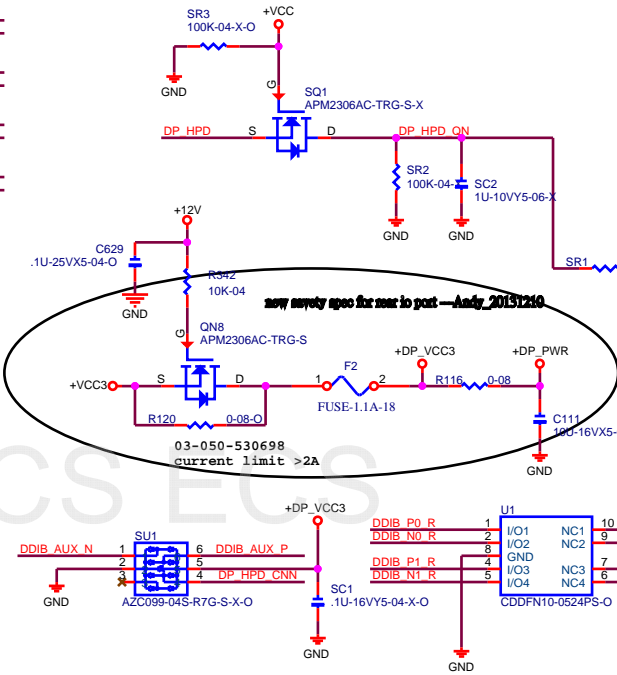
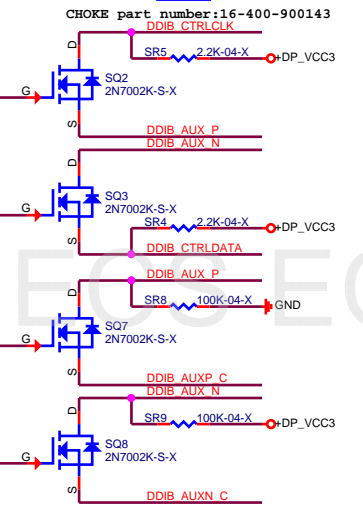
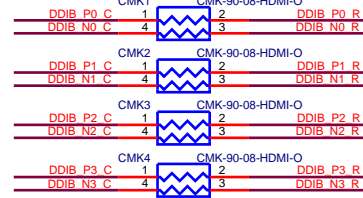
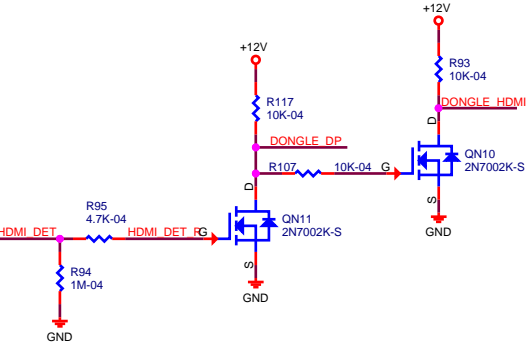
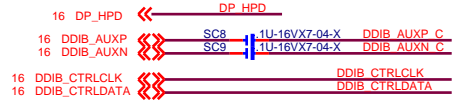
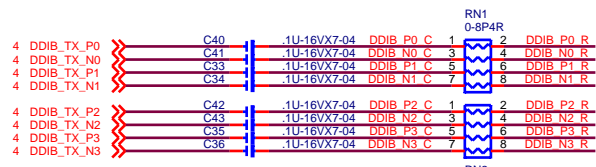


PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A

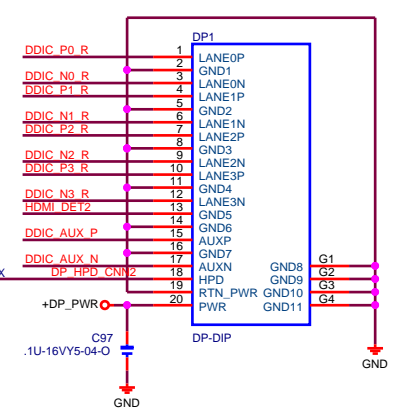
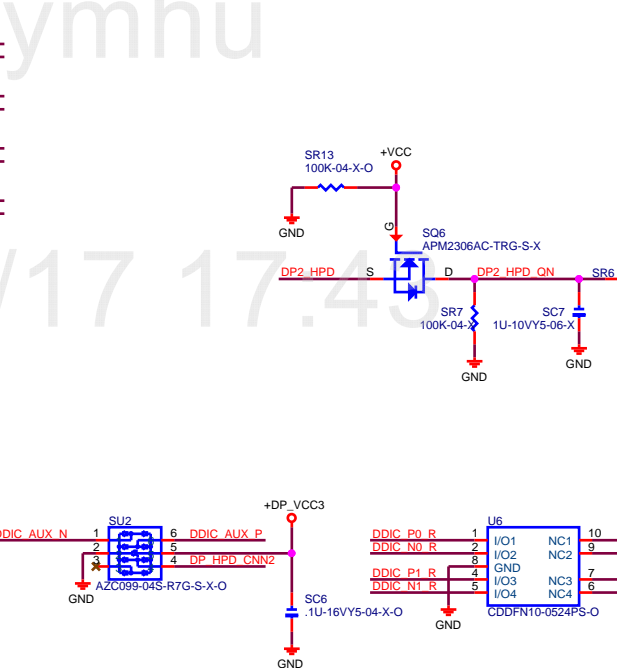
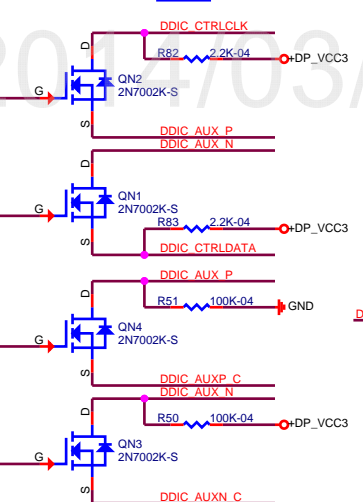
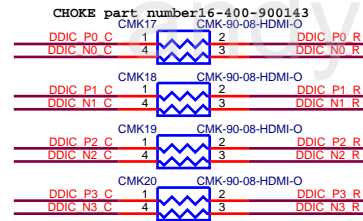
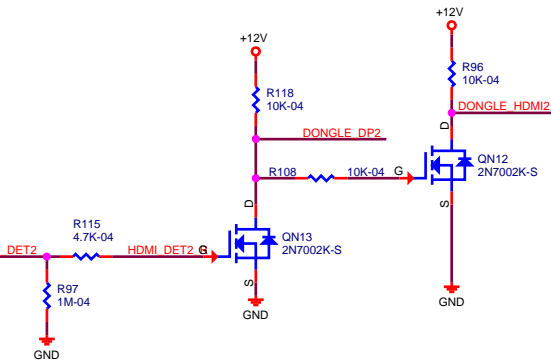
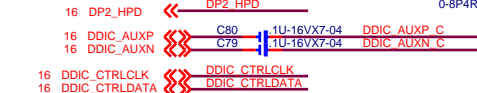
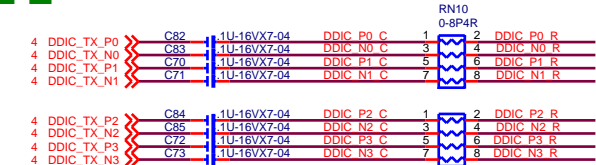


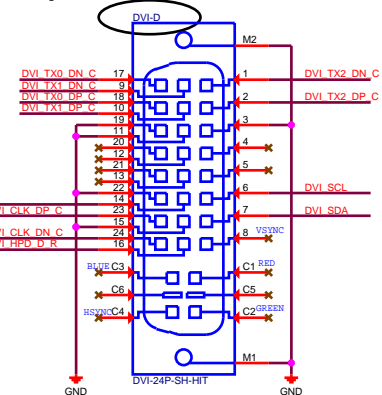
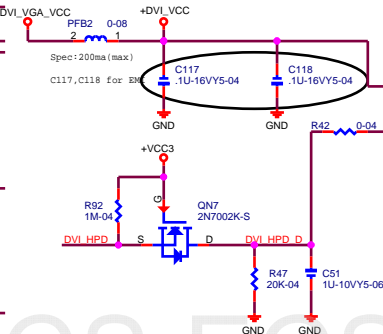
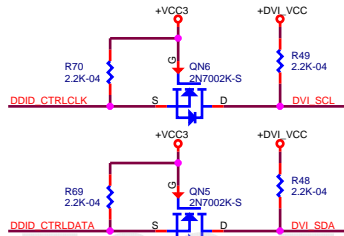
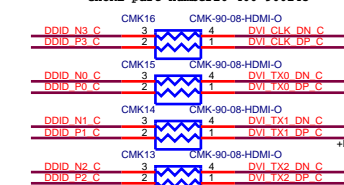
Between PCIE16 & PCIE1





DP2
DP1





U4

1 I/O1 NC1 10 DVI TX1 DN C

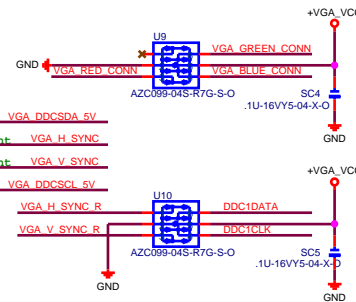
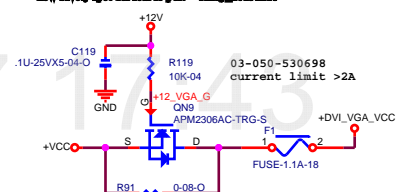
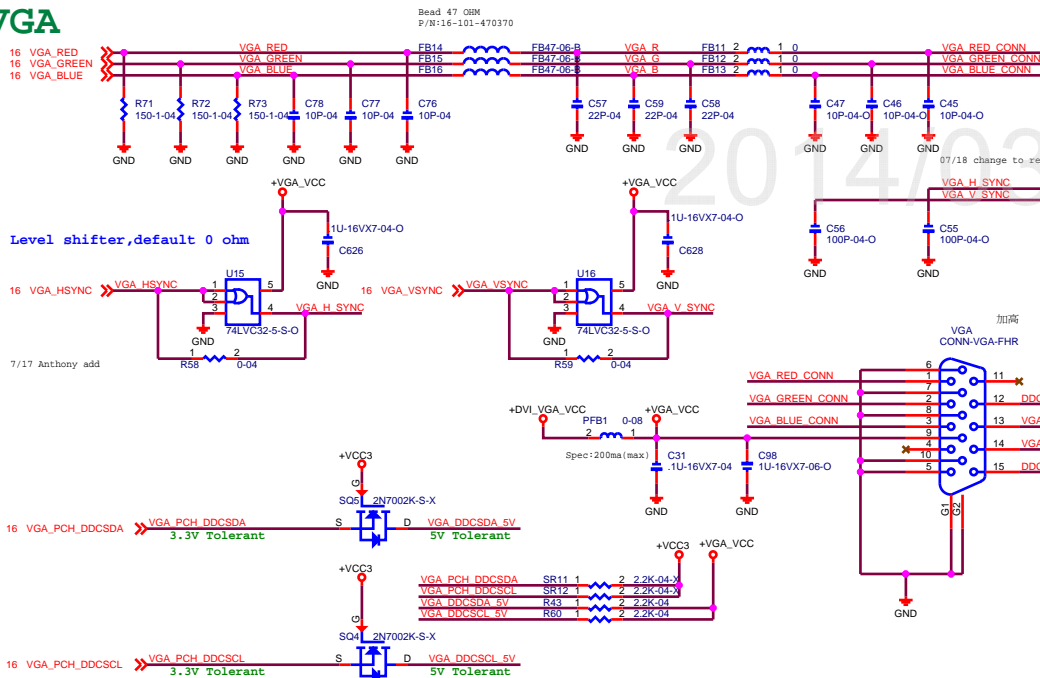
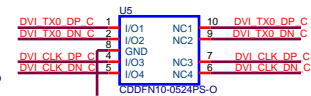
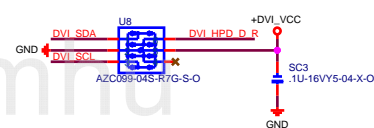
2 I/O2 NC2 9 DVI TX1 DP C

4 GND NC3 7 DVI TX2 DN C

5 I/O3 NC4 6 DVI TX2 DP C

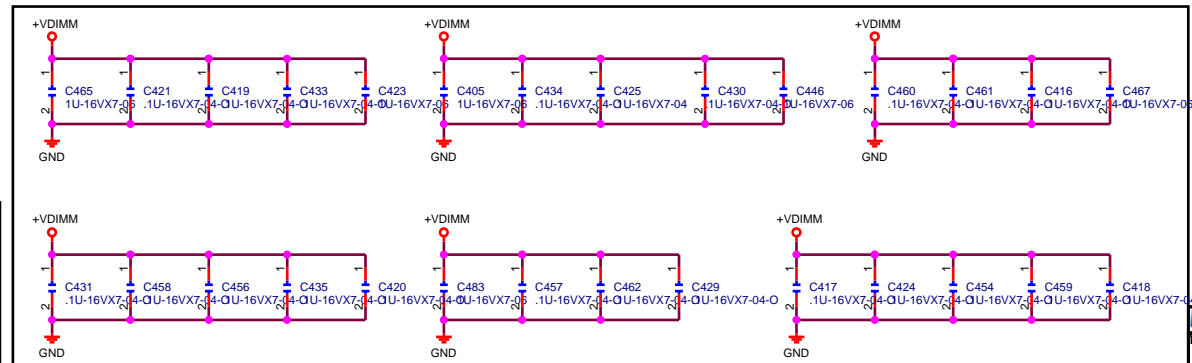
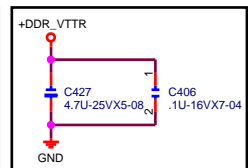
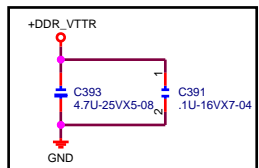
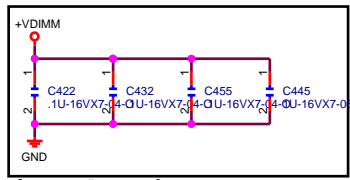
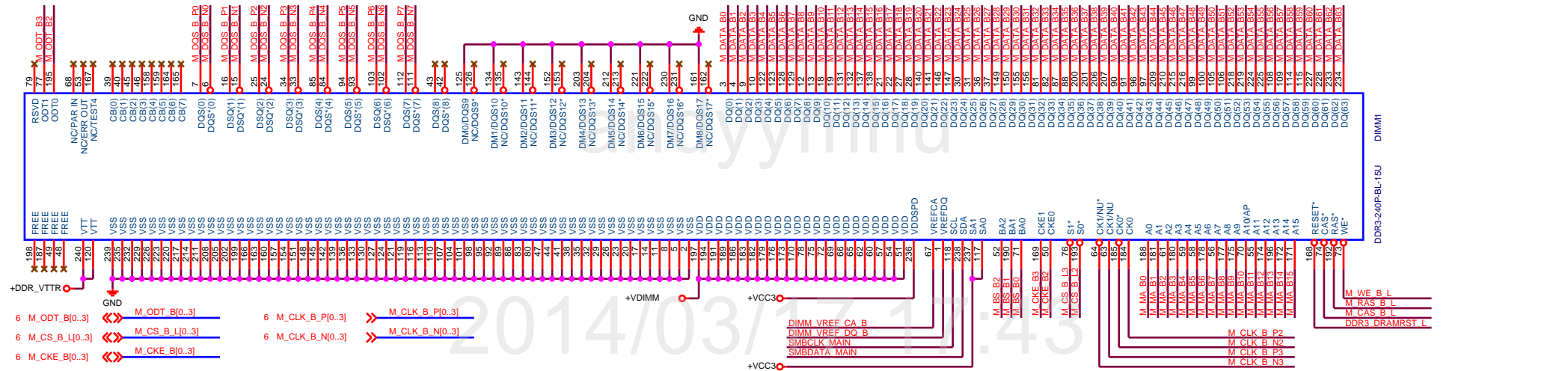
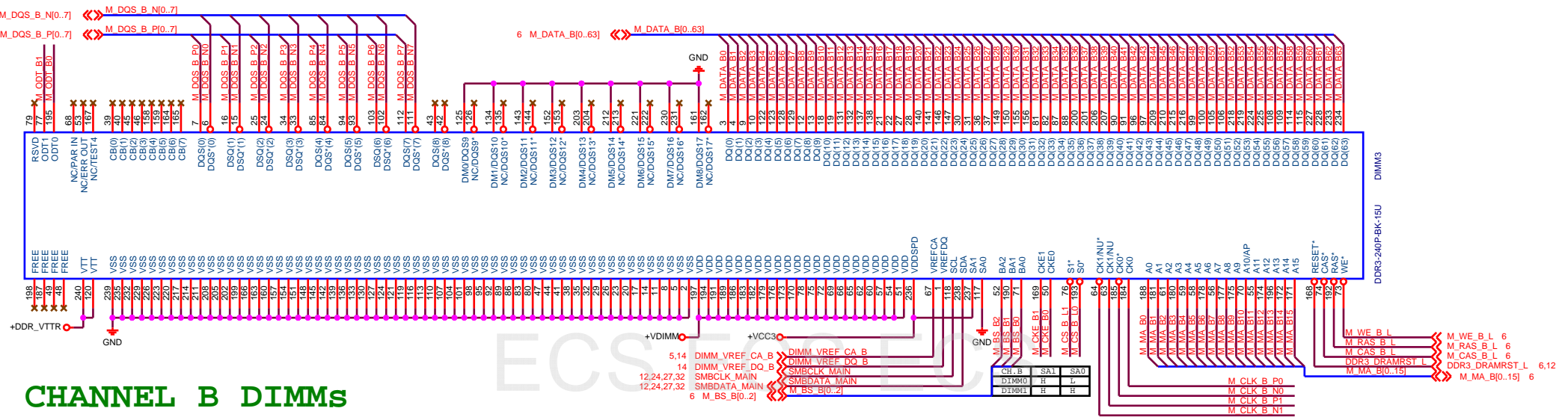
8 NC1

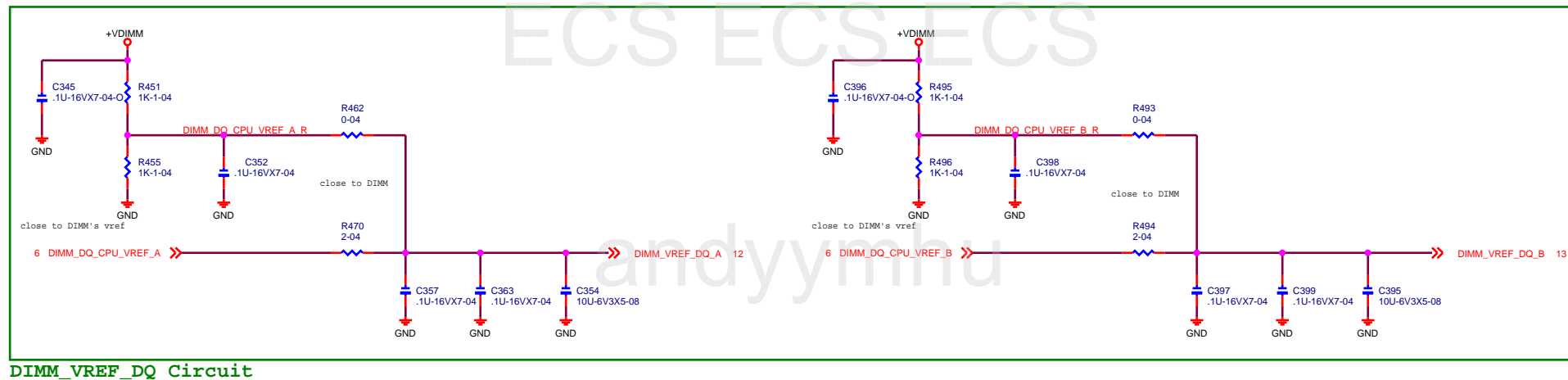
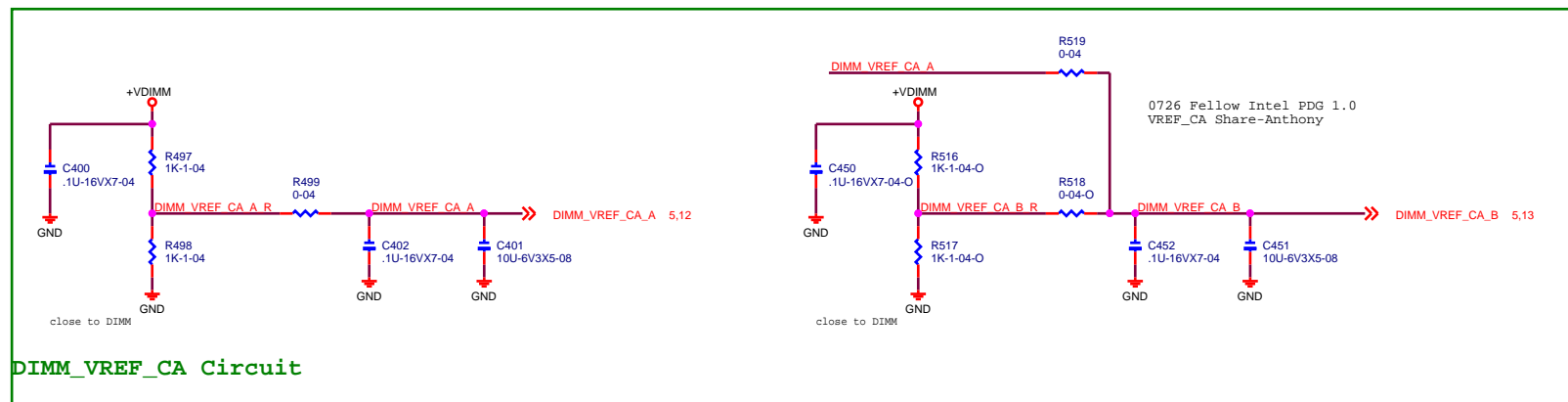
CDDFN10-0524PS-O

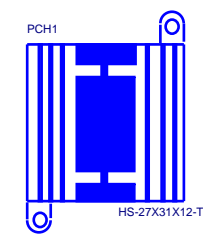
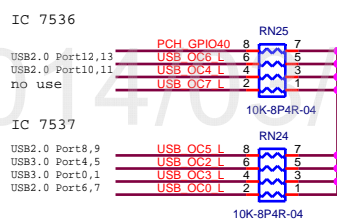
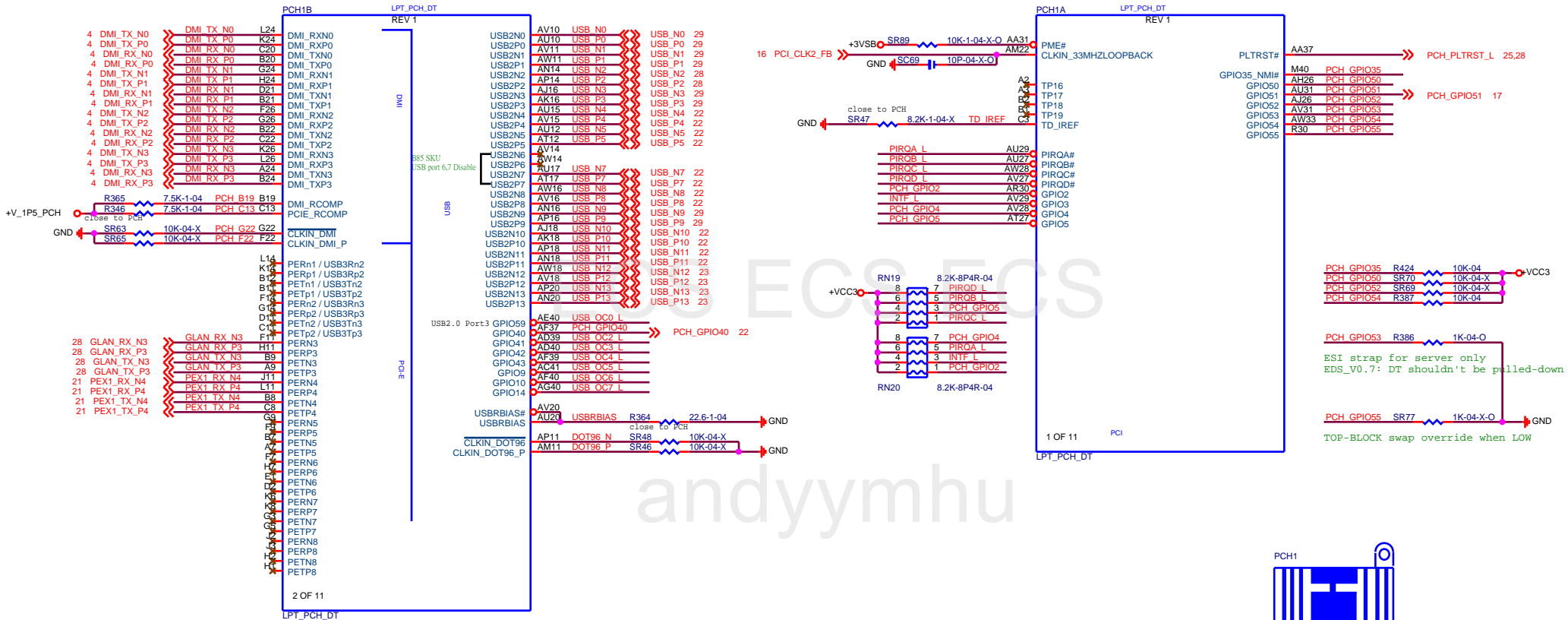


Title			
DVI-D+VGA			
Size	Customer	Document Number	Rev
		Q87H3-AD2	1.0
Date:	Monday, March 17, 2014		Sheet 11 of 40

CHANNEL B DIMMs

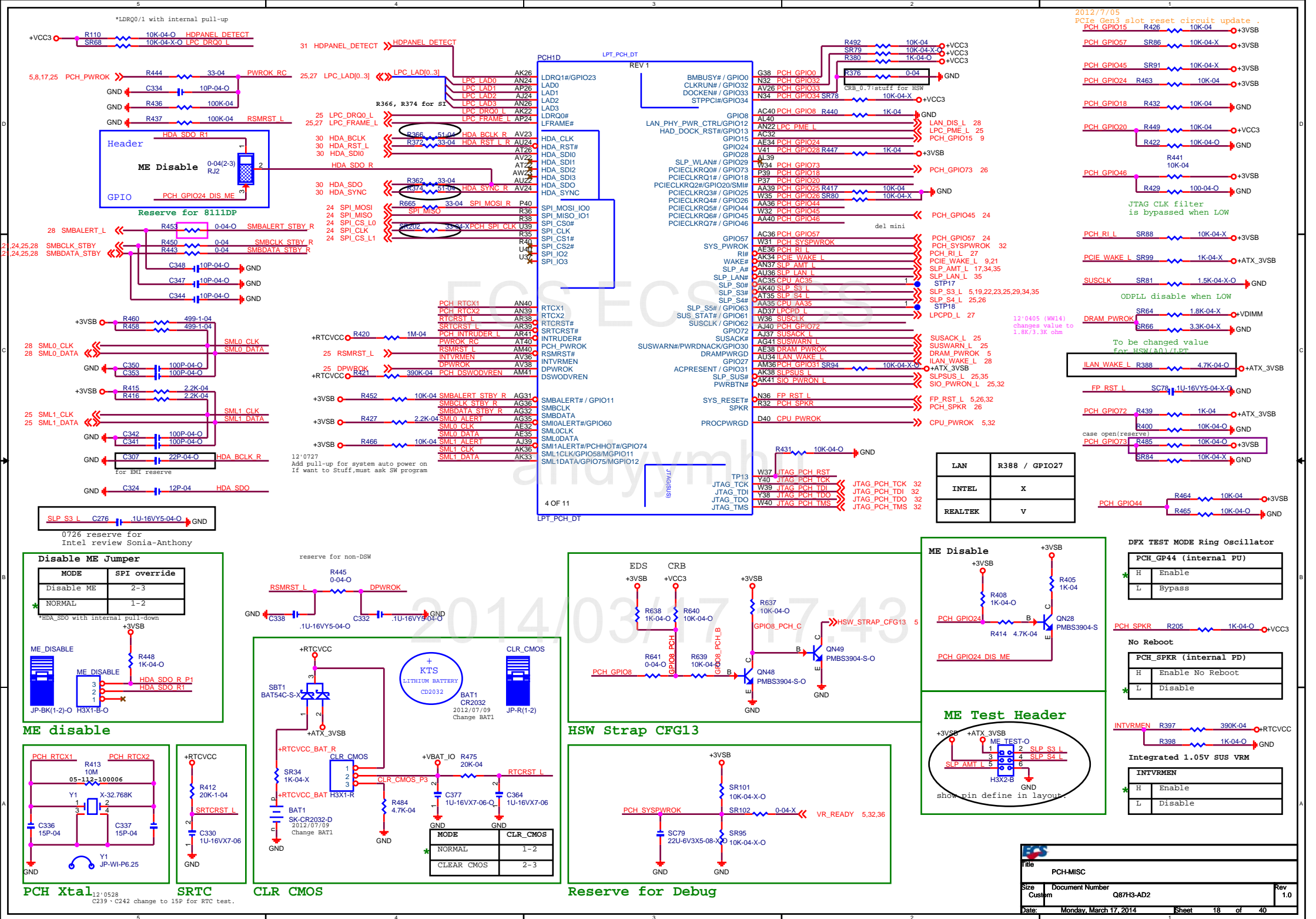


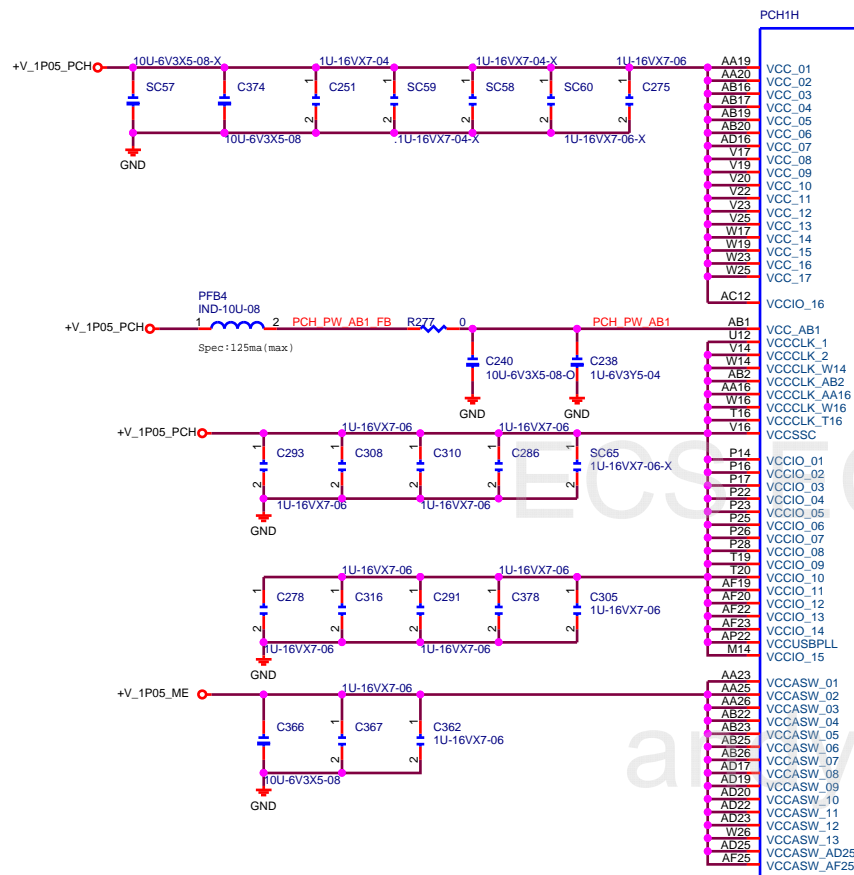




PCH heatsink (T/U phase)
 P/N: 20-120-014550
 20-120-013505

PCH chipset (SMD)
 P/N: 01D201-082640





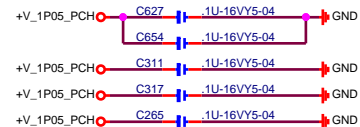
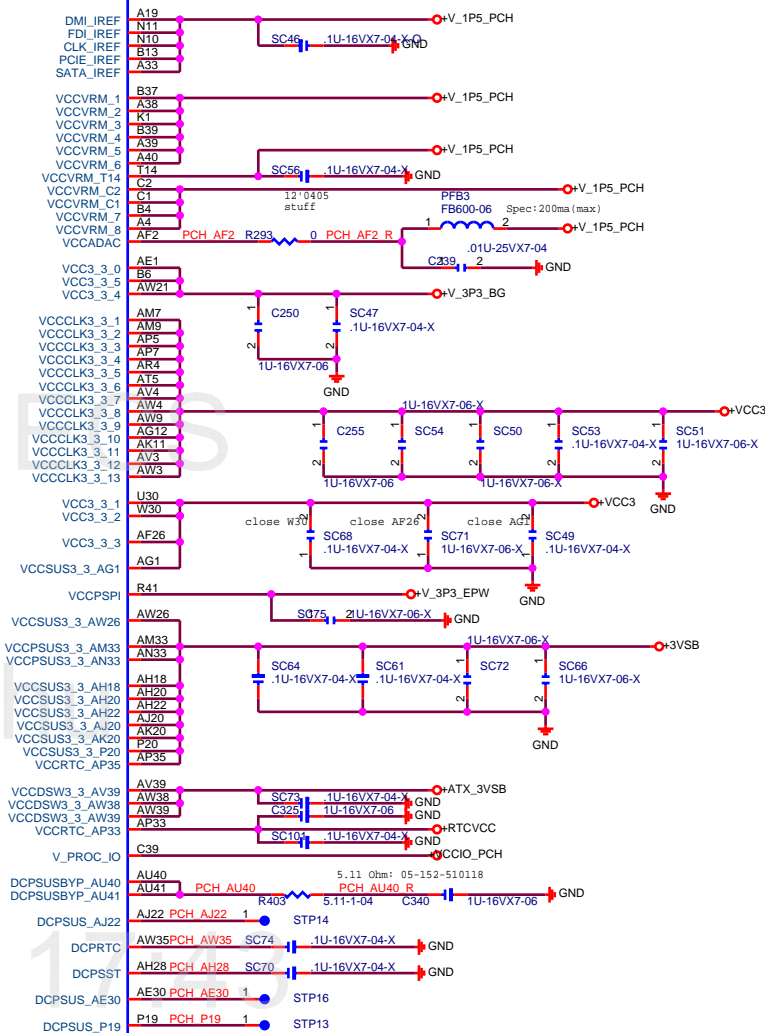
PCH1H

LPT_PCH_DT

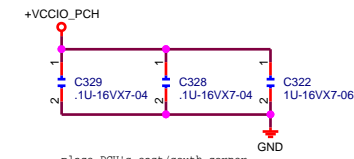
REV 1

8 OF 11

LPT_PCH_DT



stitching caps for CLK/USB3.0/PCIE/DMI/FDI around PCH

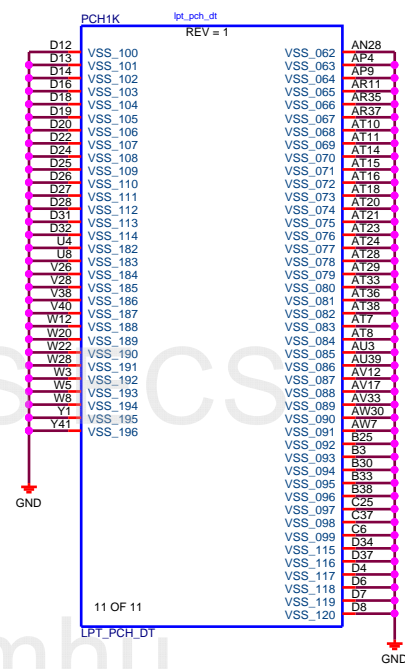
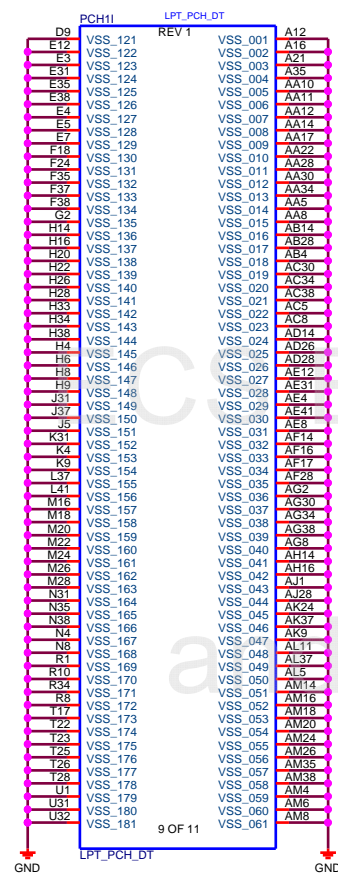
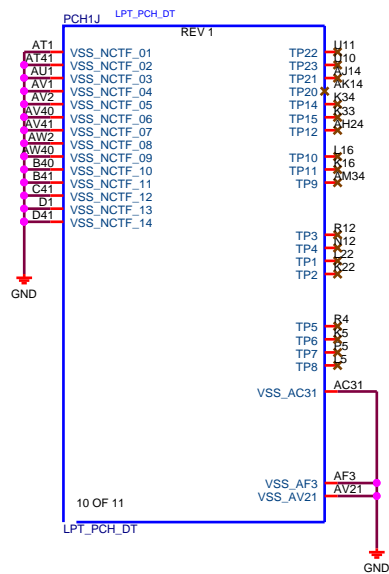


place PCH's east/south corner



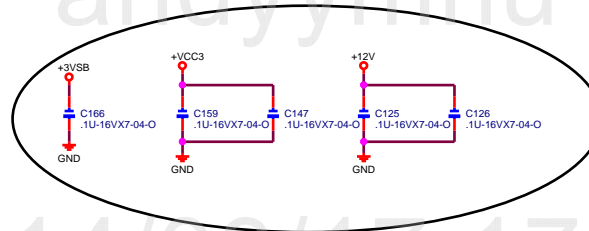
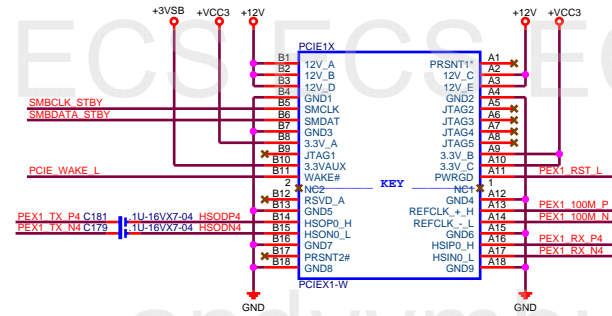
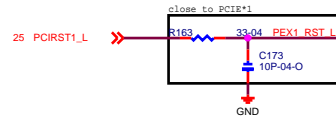
PCH-POWER		
Size	Document Number	Rev
Custom	Q87H3-AD2	1.0
Date:	Monday, March 17, 2014	Sheet 19 of 40

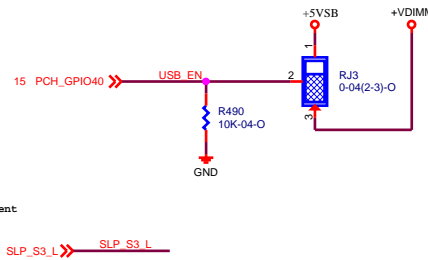
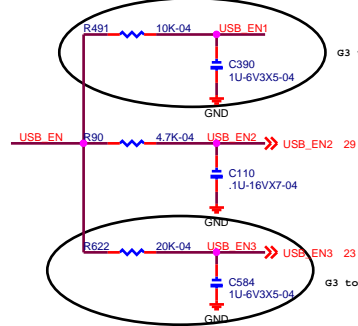
LPT EV ENG EXP



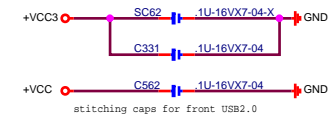
9,18,24,25,28 SMBCLK_STBY >>> SMBCLK_STBY
 9,18,24,25,28 SMBDATA_STBY >>> SMBDATA_STBY
 9,18 PCIE_WAKE_L >>> PCIE_WAKE_L

 16 PEX1_100M_P >>> PEX1_100M_P
 16 PEX1_100M_N >>> PEX1_100M_N
 15 PEX1_TX_P4 >>> PEX1_TX_P4
 15 PEX1_TX_N4 >>> PEX1_TX_N4
 15 PEX1_RX_P4 >>> PEX1_RX_P4
 15 PEX1_RX_N4 >>> PEX1_RX_N4

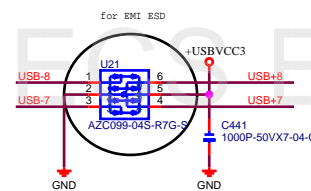
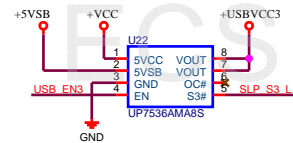
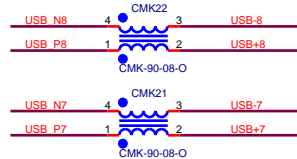
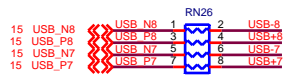




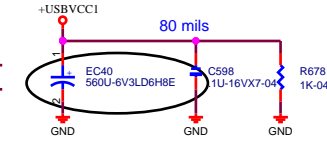
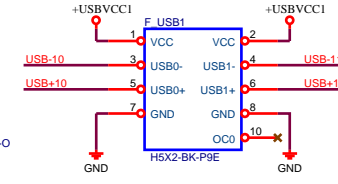
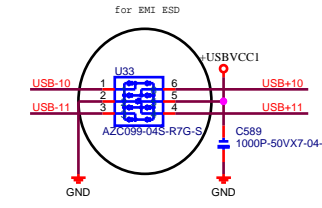
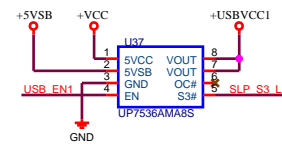
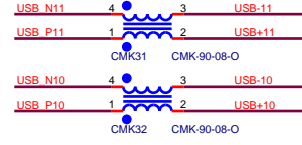
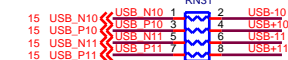
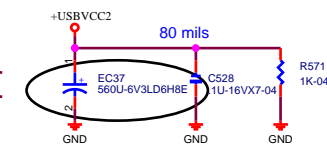
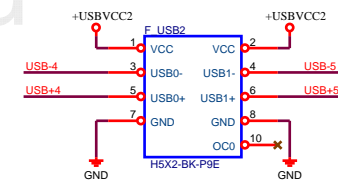
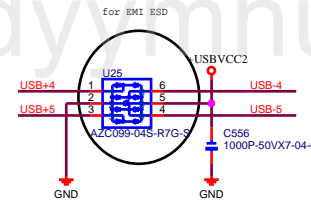
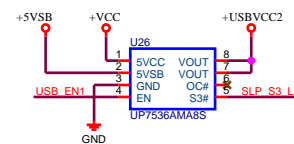
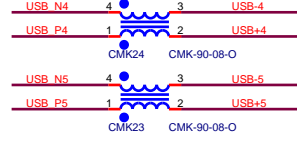
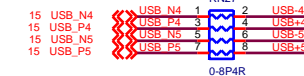
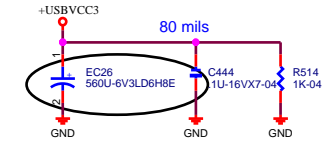
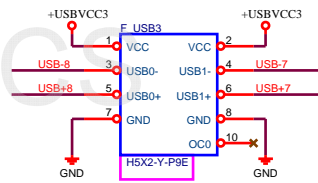
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

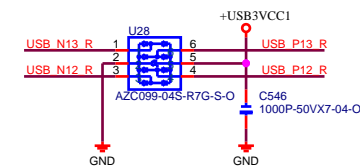
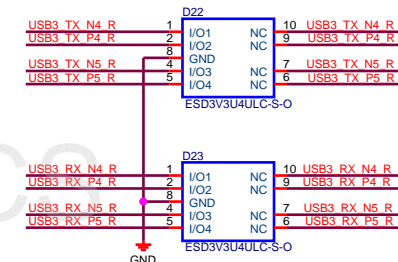
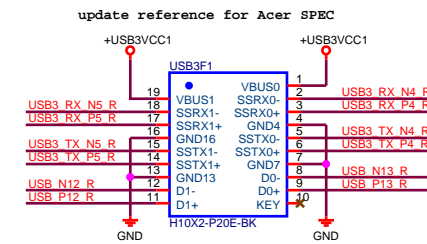
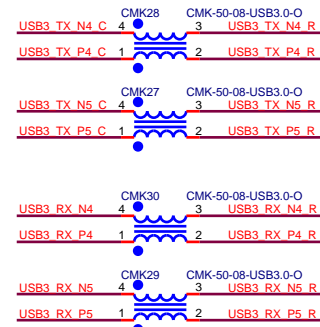


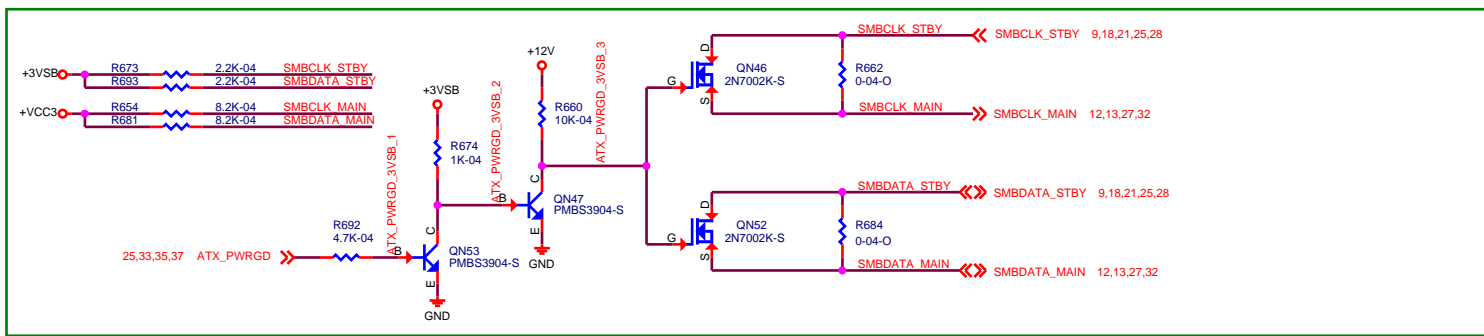
Acer EE conform all USB port not support over current protection



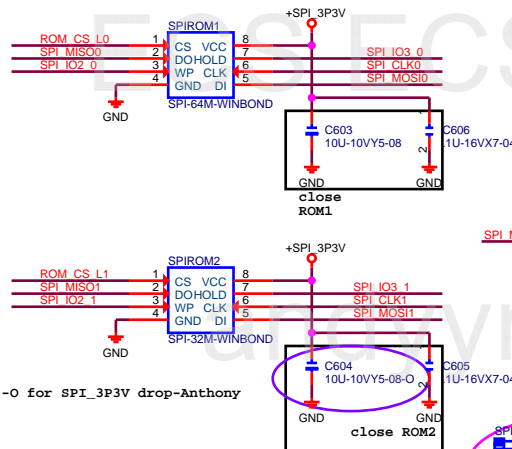
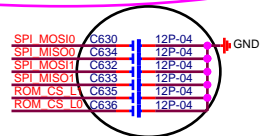
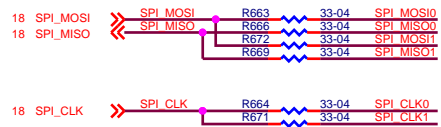
for Q87 colay B85
(B85 Disable USB port 7)
F_USB3 header 1*5 for B85 SKU



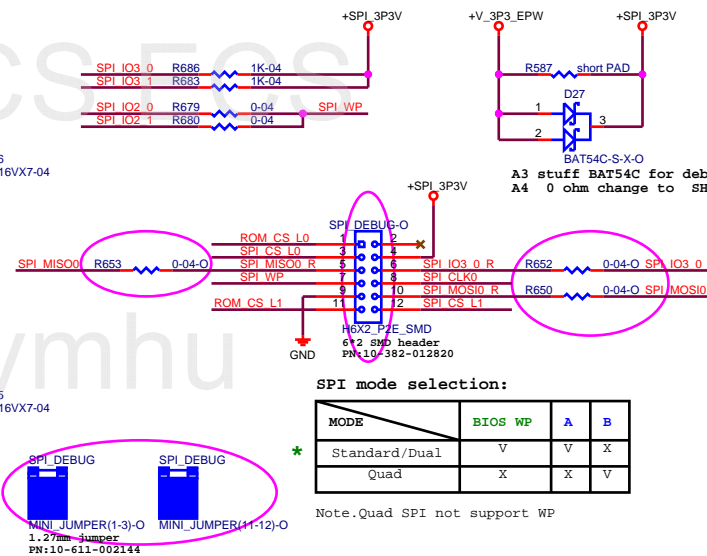




SMBus Logic Circuit



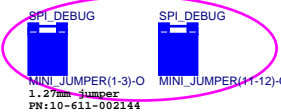
08/29 : -O for SPI_3P3V drop-Anthony



SPI mode selection:

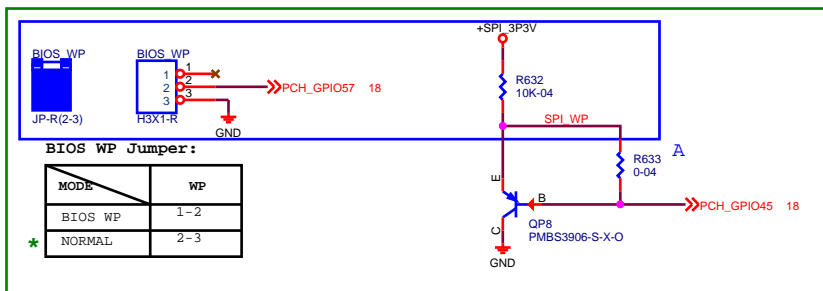
MODE	BIOS WP	A	B
Standard/Dual	V	V	X
Quad	X	X	V

Note. Quad SPI not support WP



07/18 reserve for debug only-Anthony

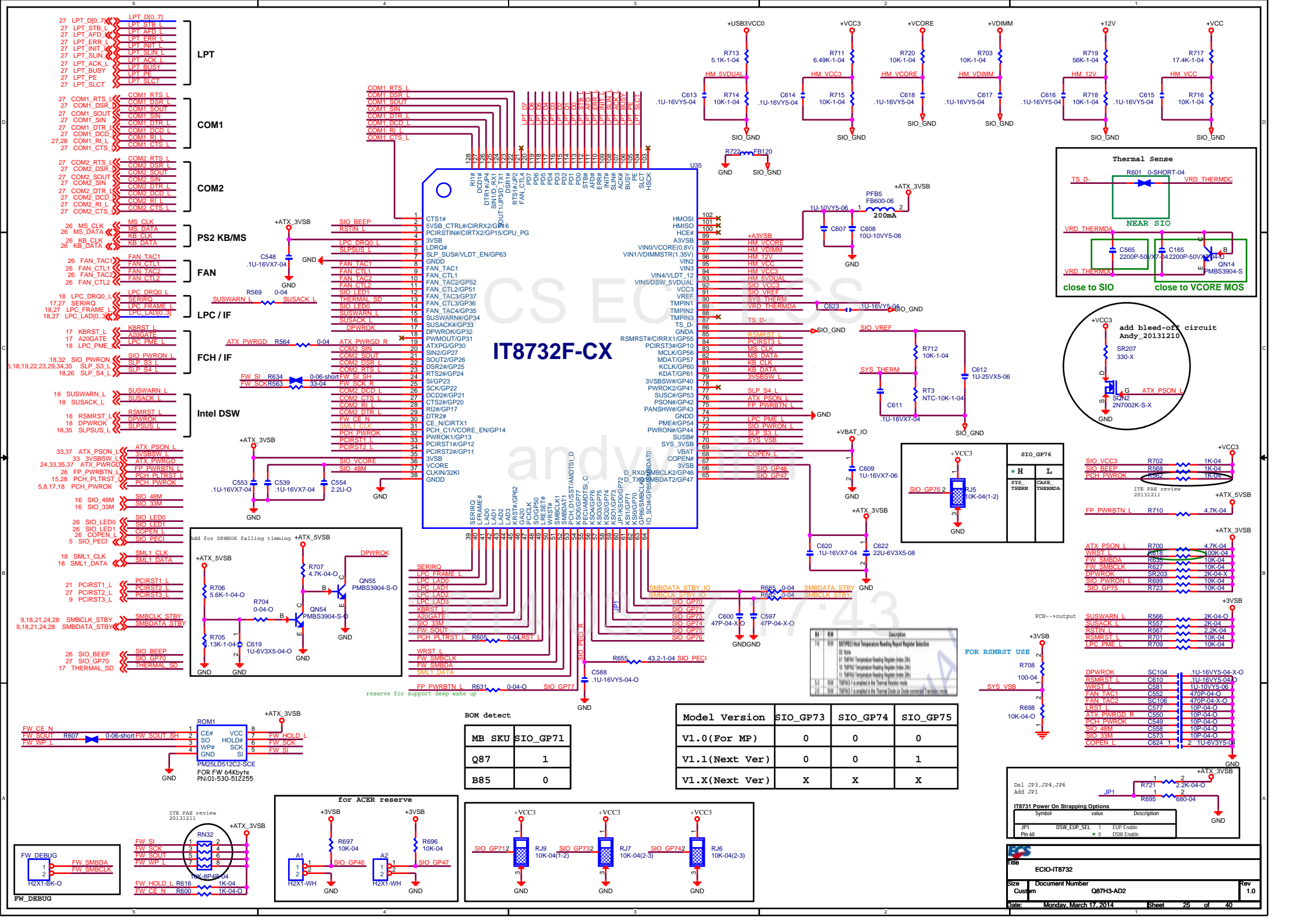
SPI ROM

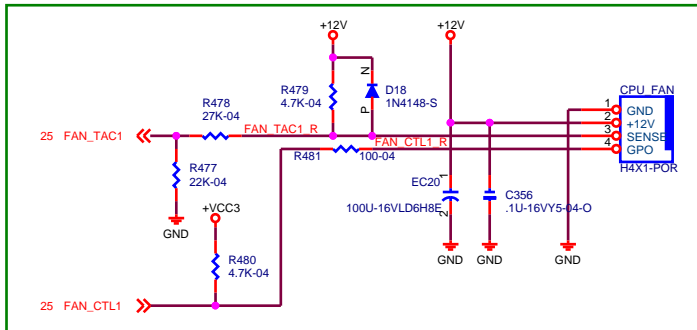


BIOS WP

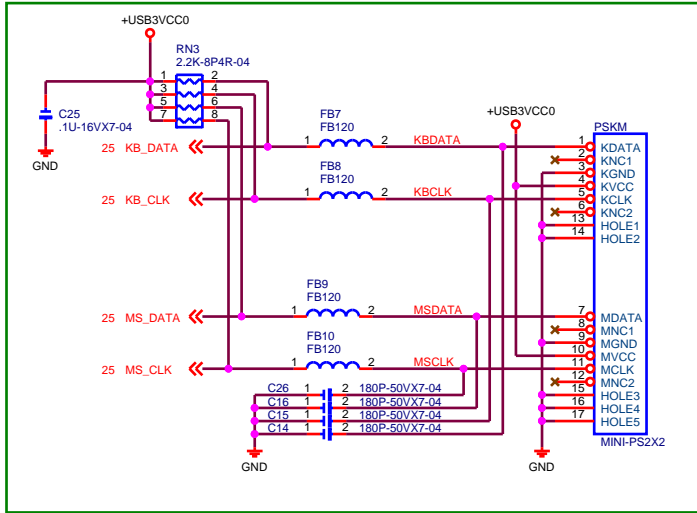
BIOS WP Jumper:

MODE	WP
BIOS WP	1-2
NORMAL	2-3

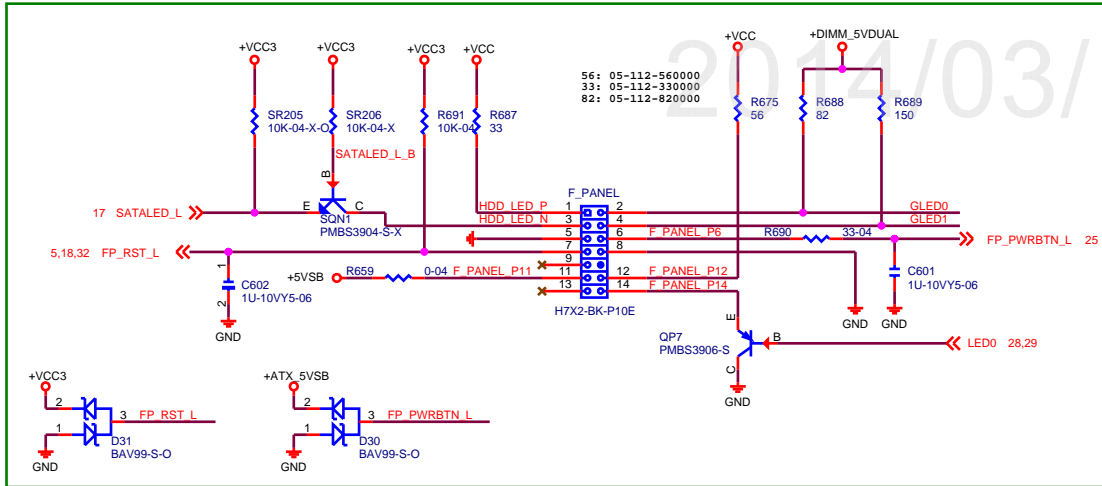




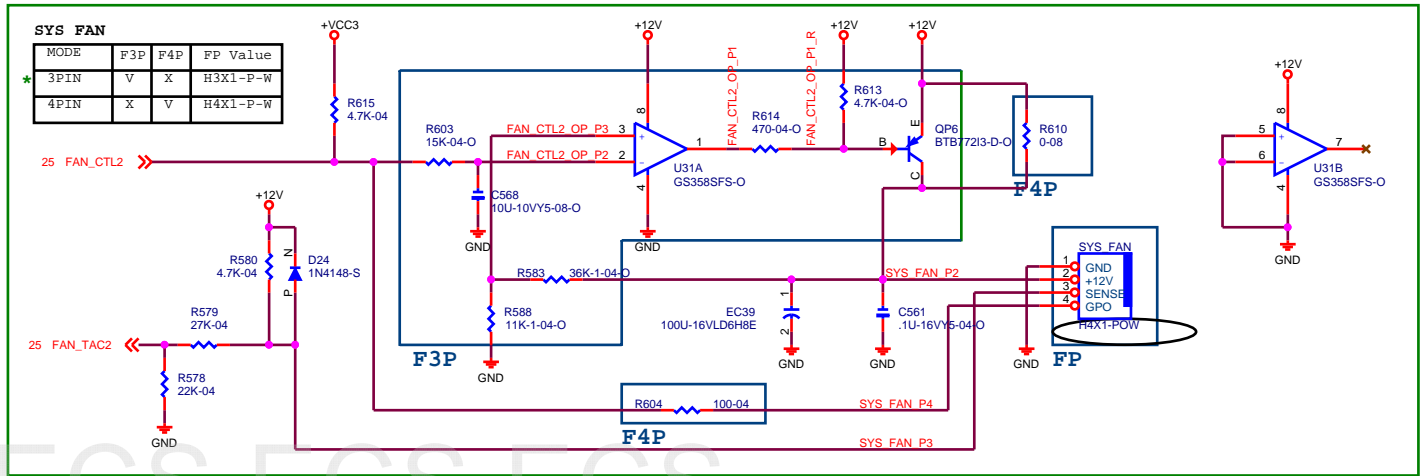
CPU_FAN 4 pin circuit



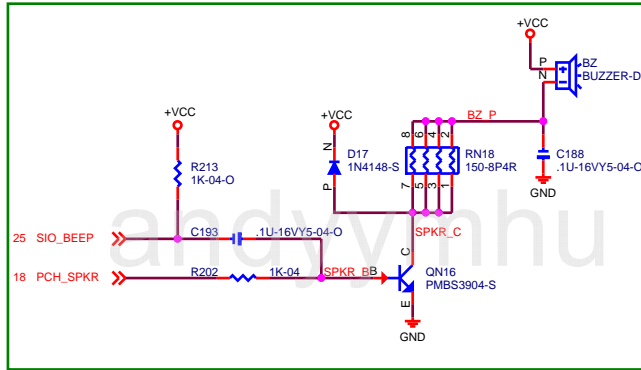
PS2 circuit



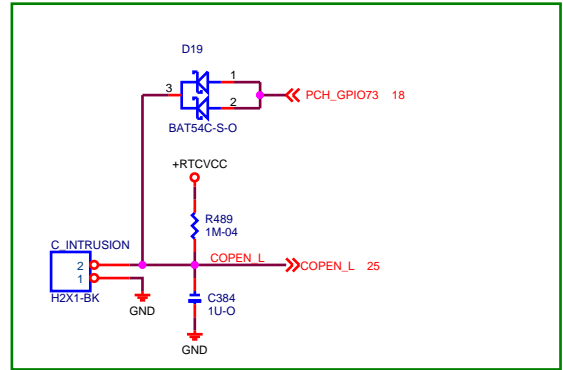
Front Panel circuit



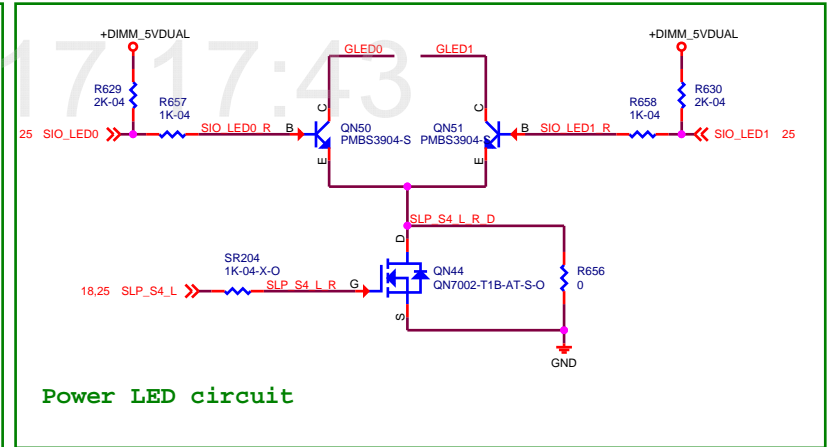
SYS_FAN 3/4 pin co-layout circuit



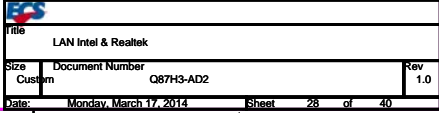
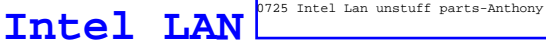
Buzzer circuit

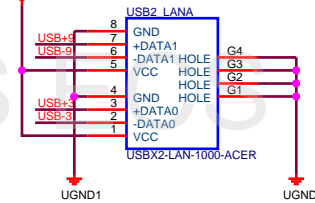
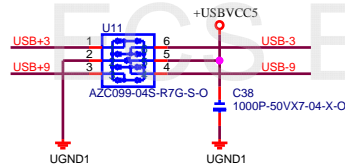
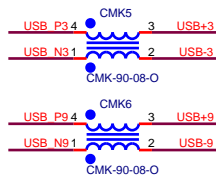


Case open circuit

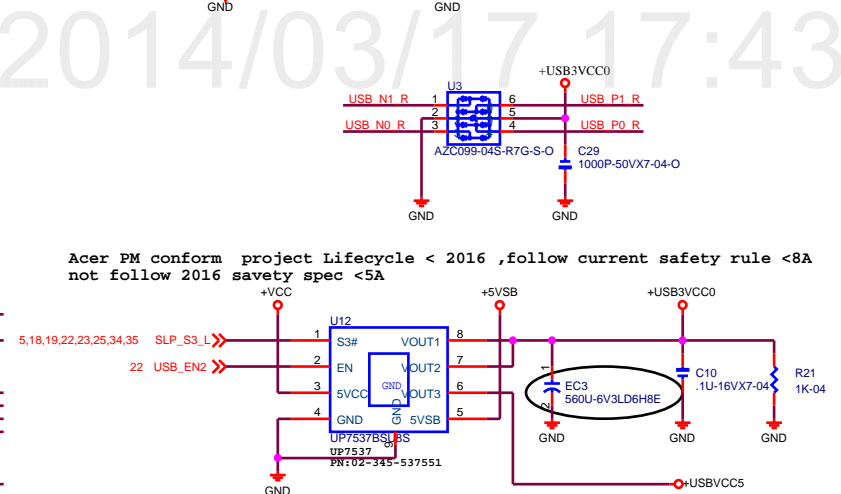
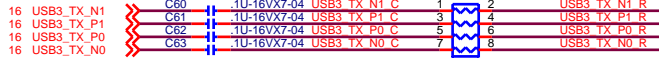
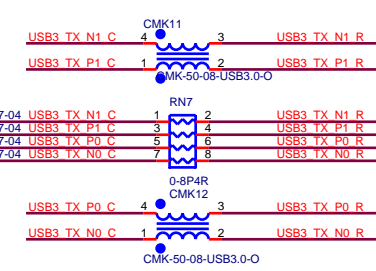
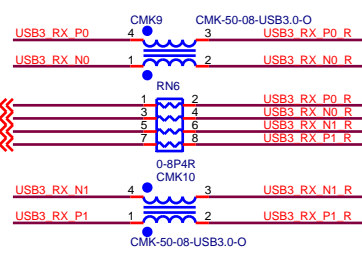
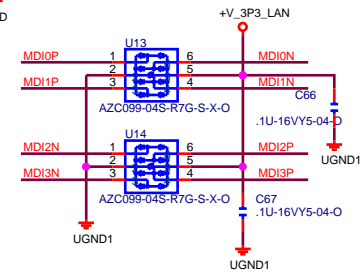
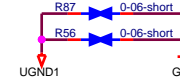
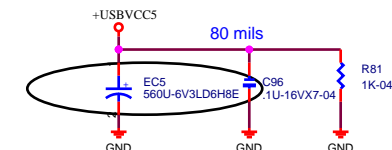
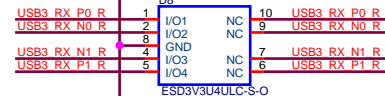
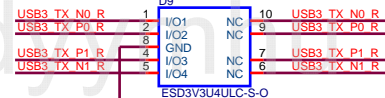
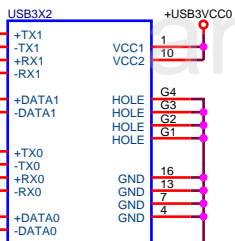
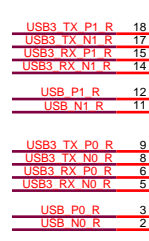
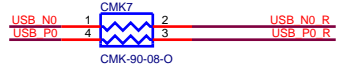
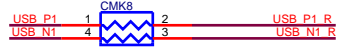


Power LED circuit

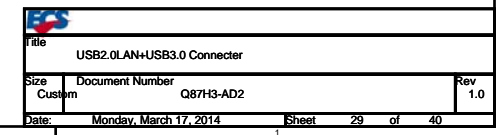
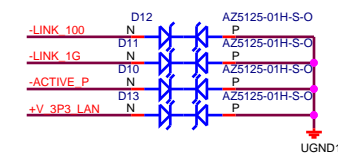


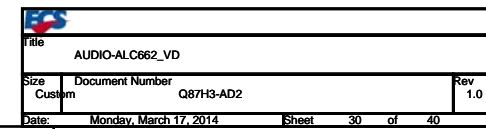
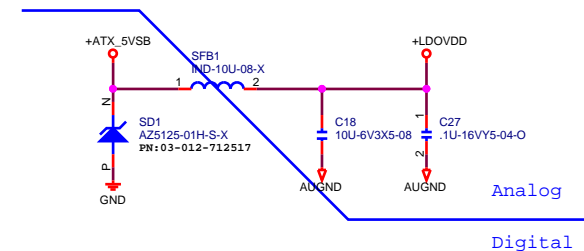


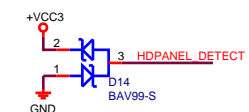
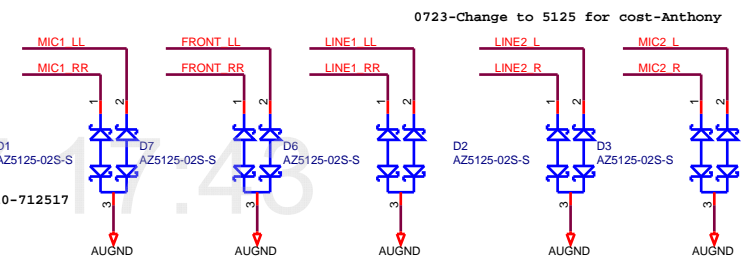
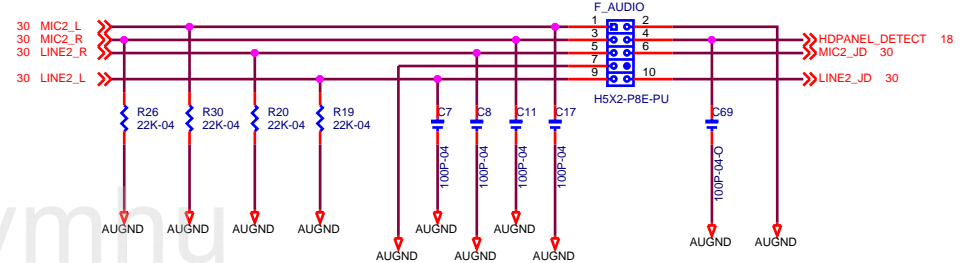
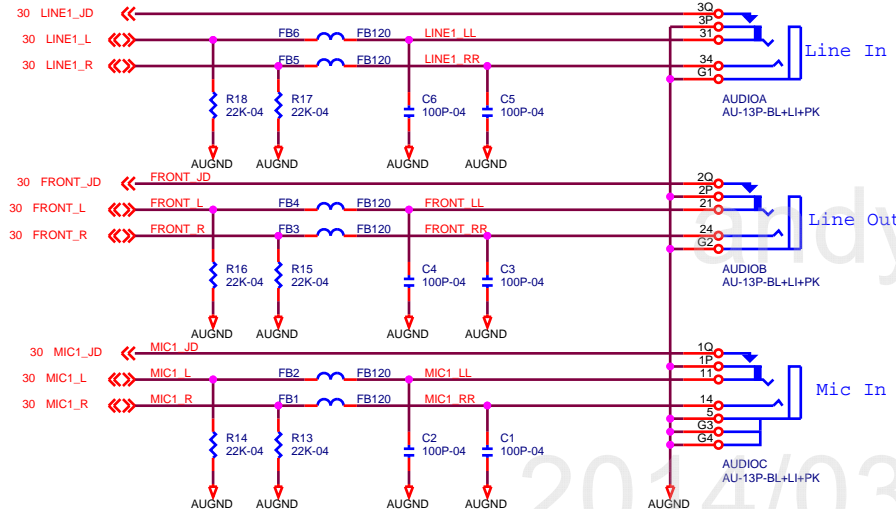
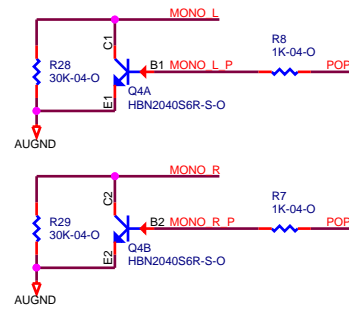
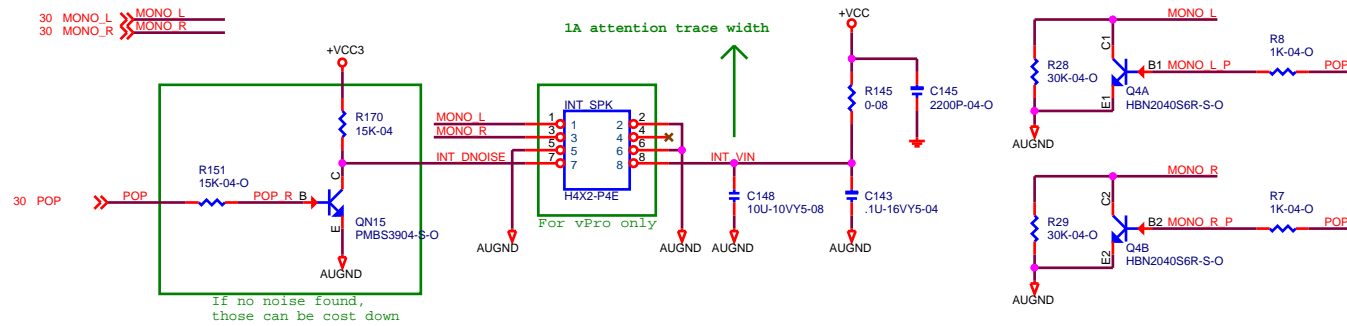
update reference for Acer SPEC



Acer PM conform project Lifecycle < 2016 ,follow current safety rule <8A
not follow 2016 savety spec <5A





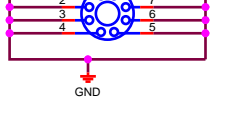
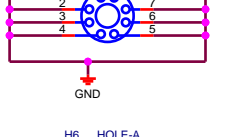
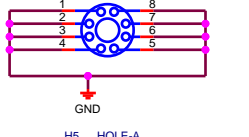
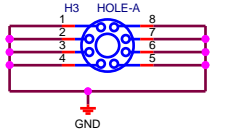
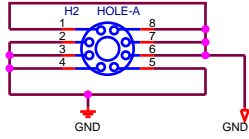
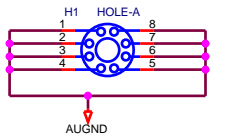


A	B	C
	PIN	FUNCTION
LINE IN	3Q	LINE IN-JD
	3P	AUGND
	31	LINE IN_L
	34	LINE IN_R
	G1	AUGND
LINE OUT	2Q	LINE OUT-JD
	2P	AUGND
	21	LINE OUT_L
	24	LINE OUT_R
	G2	AUGND
MIC IN	1Q	MIC IN-JD
	1P	AUGND
	11	MIC IN_L
	14	MIC IN_R
	5	AUGND

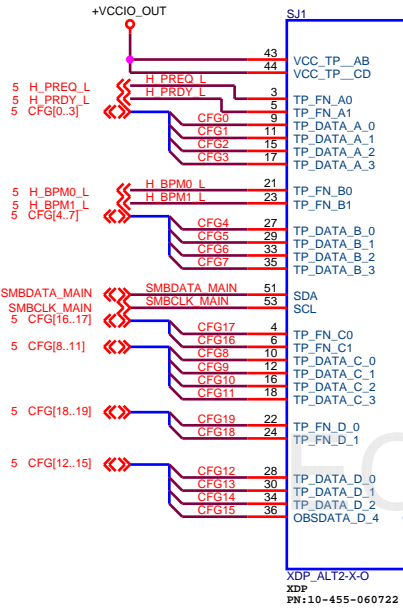
AZ5125-02S , PN:03-010-712517

0815-Acer confirm remove JD TVS

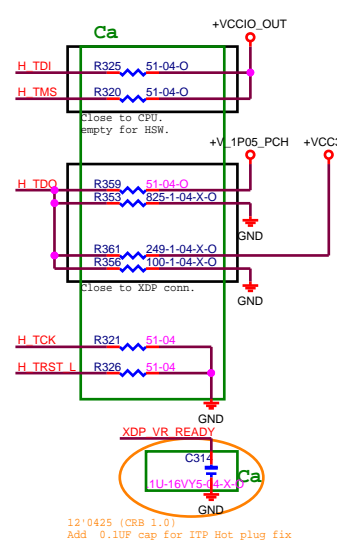
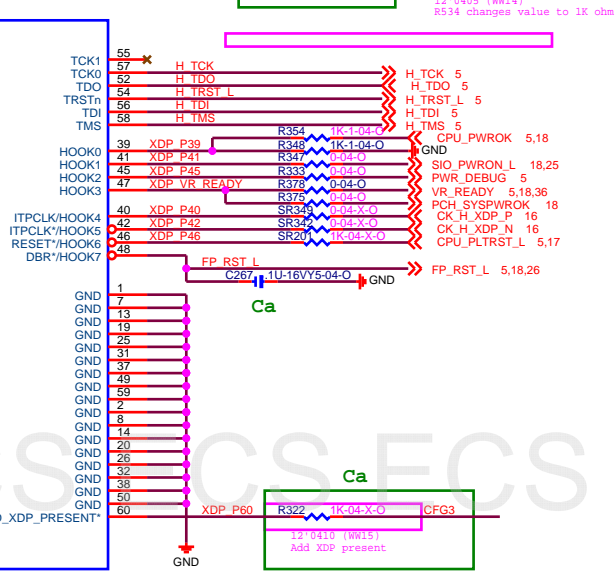
BAV99-S , PN:03-030-709941



07/20 change to stuff for OC-Anthony

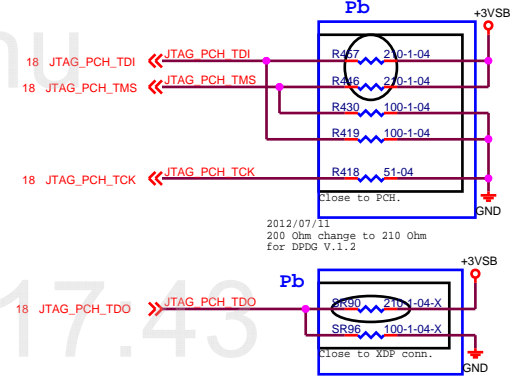


XDP
PN:10-455-060722



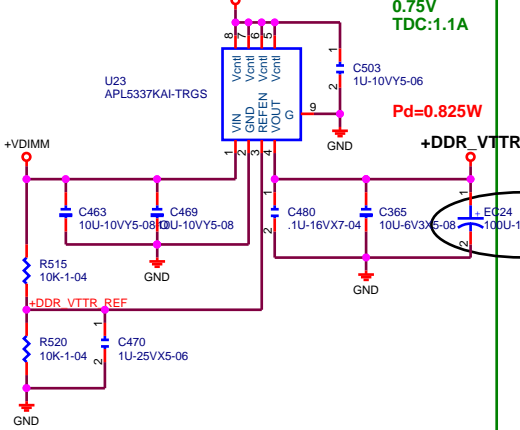
	Ca
CPU XDP function	V
NO CPU XDP function	X

-O: 0.1uF

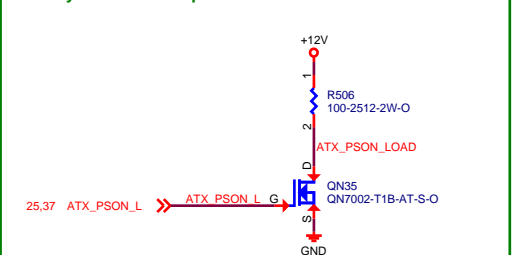


	Pb
PCH XDP function	V
NO PCH XDP function	X

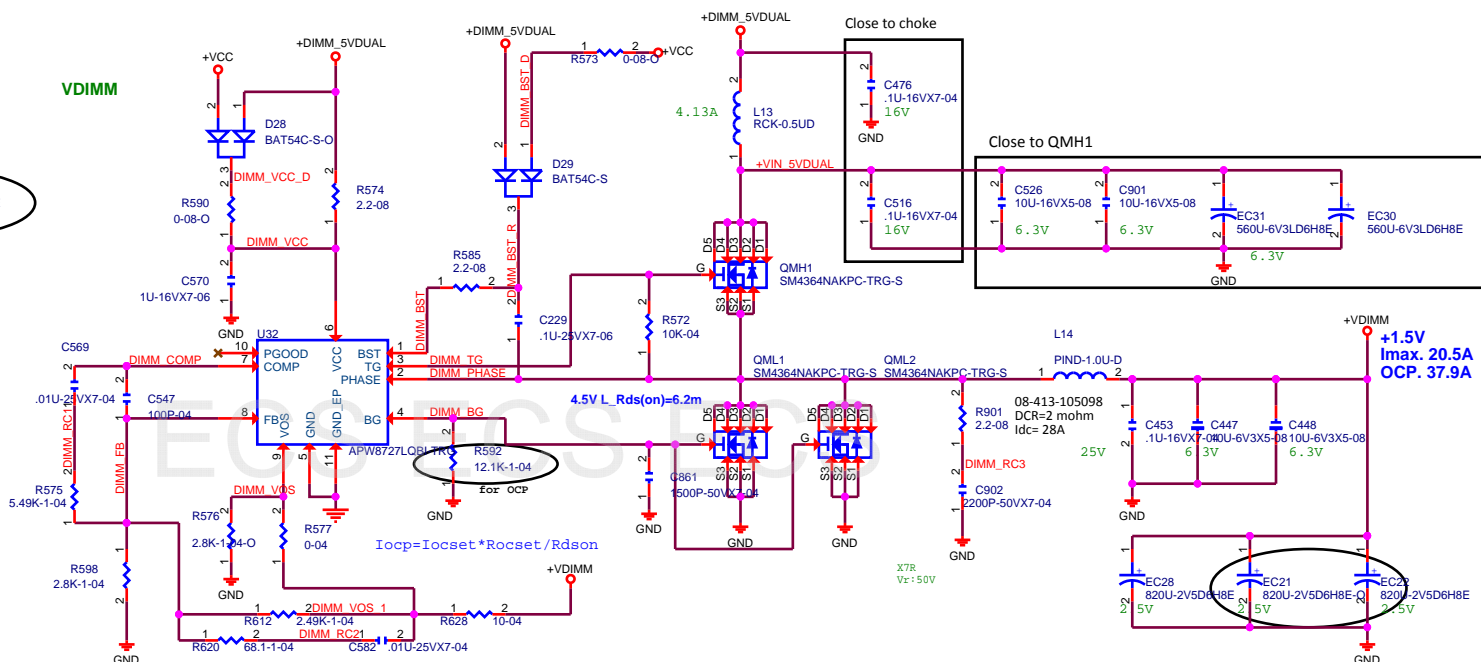
DDR VTT



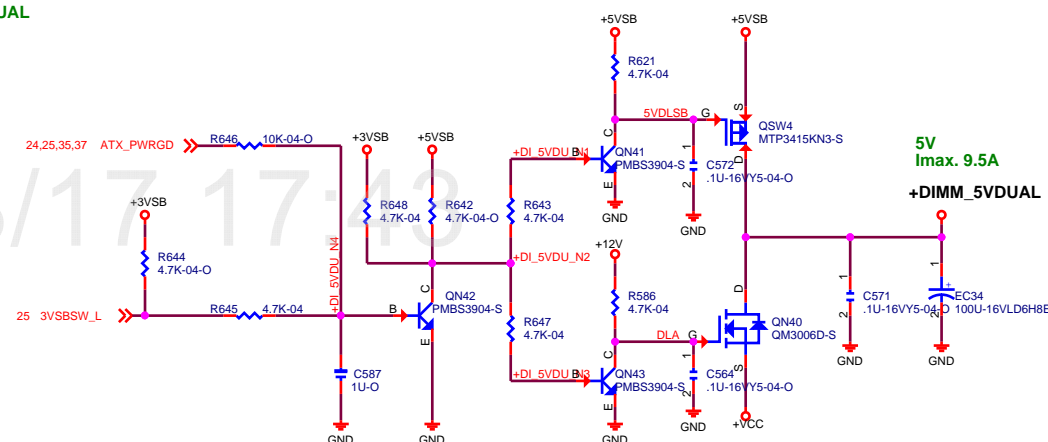
Dummy Load for ATX power



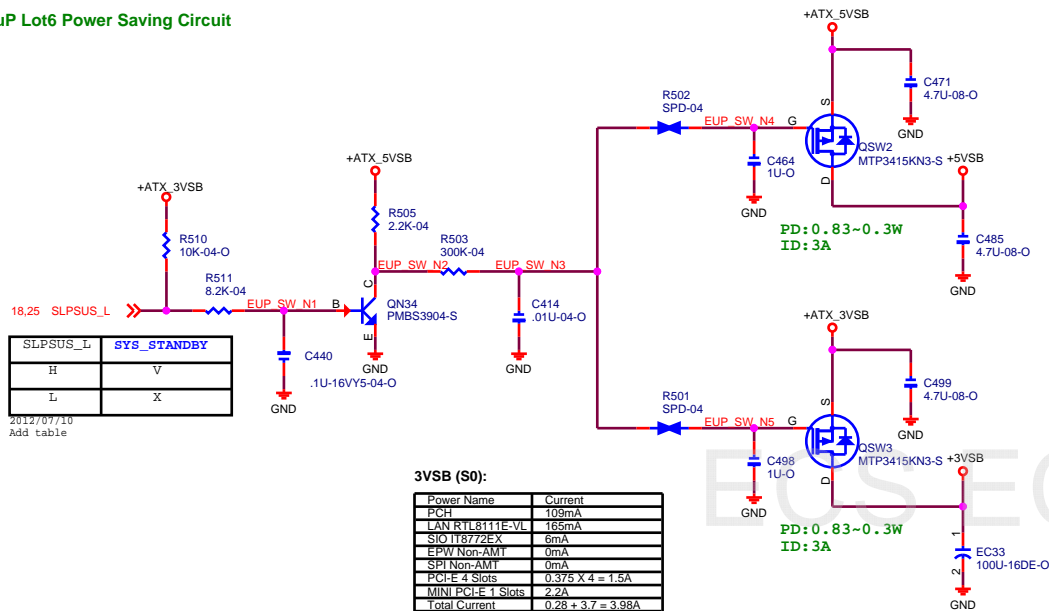
VDIMM



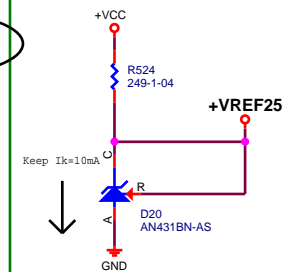
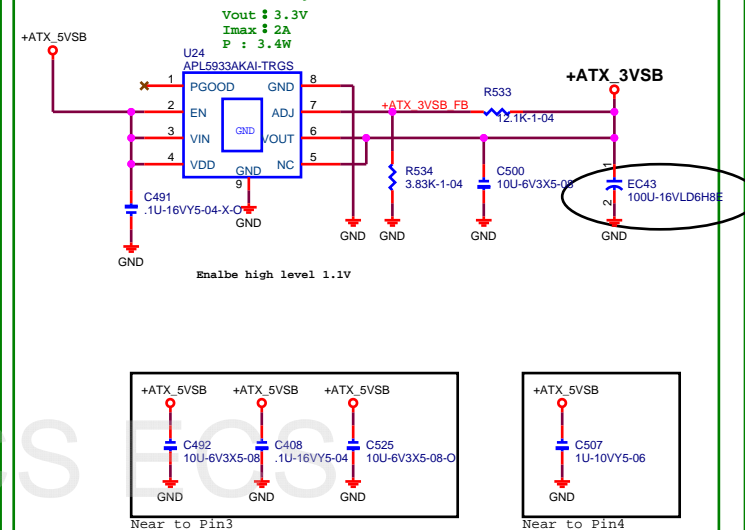
5VDUAL



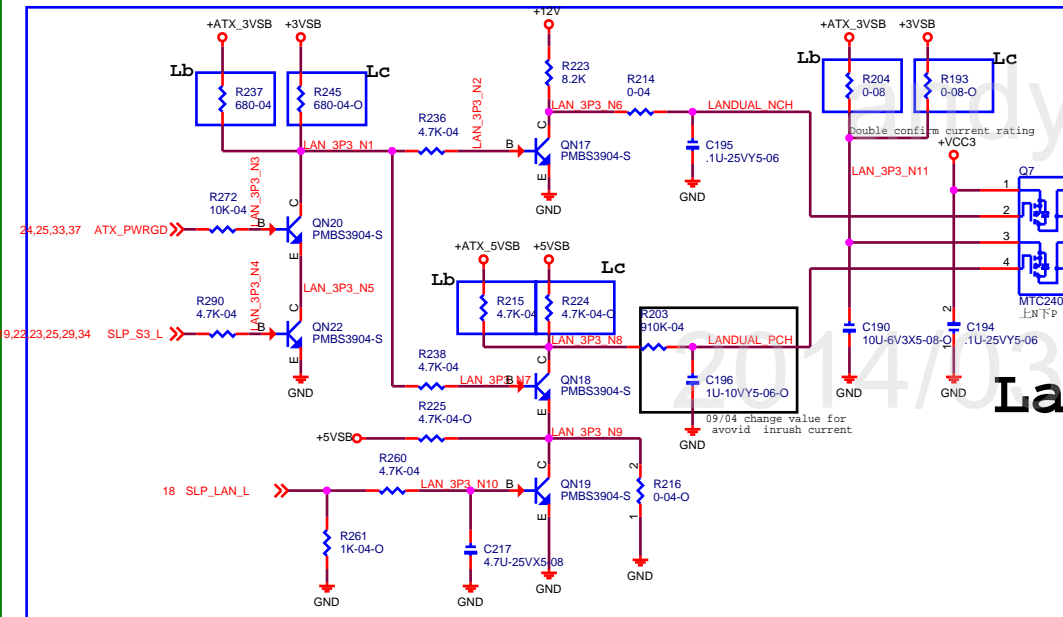
EuP Lot6 Power Saving Circuit



+3V Standby



LAN Power Circuit



LAN Power Source

	SUP Enable Q3-->S5,S5	La	Lb	Lc	Ld	Le
Intel LAN	can wake up	V	V	X		
	can't wake up	V	X	V		
Realtek LAN	can wake up				V	X
	can't wake up				X	V

SPI ROM & PCH Power Circuit

